FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16506-1E

32-bit Microcontroller

CMOS

FR60Lite MB91230 Series

MB91233L/MB91F233/MB91F233L/MB91V230

■ DESCRIPTION

The MB91230 series is a line of standard microcontrollers, based on a 32-bit high-performance RISC CPU and containing variety of I/O resources, for embedded control applications which require high CPU performance at high speed processing.

Audio motor control storage : Designed to specifications for embedded control applications which high CPU performance power processing.

The MB91230 series belongs to the FR60Lite family.

■ FEATURES

- 32-bit RISC, load/store architecture with a 5 stage pipeline
- Maximum operating frequency: 33.6 MHz (oscillation frequency = 4.2 MHz, oscillation frequency 8-multiplier (PLL clock multiplication method))
- 16-bit fixed length instructions (basic instructions)
- Execution speed of instructions : 1 instruction per cycle

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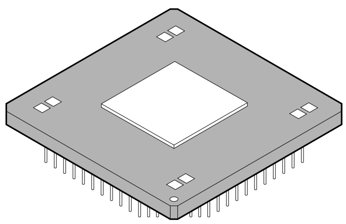
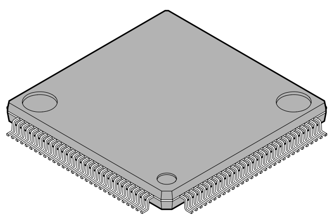
■ PACKAGES

401-pin Ceramic PGA



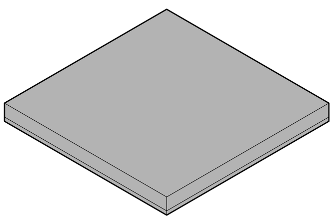
(PGA-401C-A02)

120-pin Plastic LQFP



(FPT-120P-M05)

128-pin plastic FLGA



(LGA-128P-M01)

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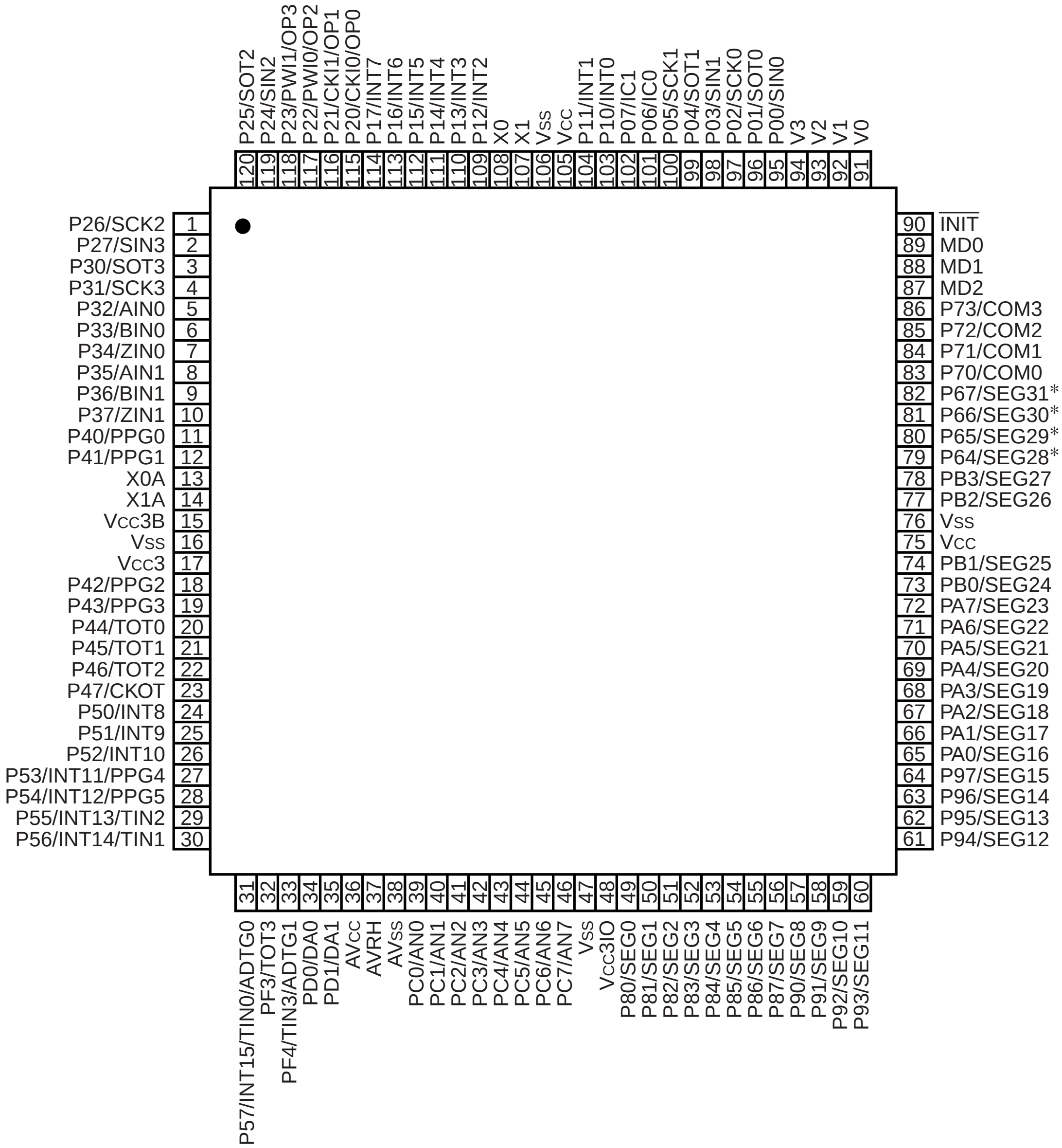
- Memory-to-memory transfer, bit handling, and barrel shift instructions, etc. : Instructions suitable for embedded applications
- Function entry/exit instructions, multiple-register load/store instructions : Instructions adapted for C-language
- Register interlock function : Facilitates coding in assembler
- Built-in multiplier with instruction-level support
  - 32-bit multiplication with sign : 5 cycles
  - 16-bit multiplication with sign : 3 cycles
- Interrupt (PC and PS save) : 6 cycles (16 priority levels)
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction compatible with FR family
- Capacity of built-in ROM and ROM type
  - MASK ROM : 256 KB
  - FLASH ROM : 256 KB
- Capacity of built-in RAM : 16 KB
- General-purpose ports : Maximum 98 ports (including N-ch open-drain port : 4 ports)
- A/D converter (series-parallel type)
  - Resolution : 10-bit : 8 ch (4 ch × 2 unit)
  - Conversion time : 1.69 µs (Minimum conversion time)
- D/A converter (R-2R type)
  - Resolution : 8-bit : 2 ch (independence)
  - Conversion speed : 0.6 µs (when load capacitance 20 pF)
- External interrupt input : 16 ch
- Bit search module (for REALOS)
  - Function for searching the MSB (Upper bit) in each word for the first “0” or “1” inverted point
- UART (full-duplex double buffer) : 4 ch
  - Selectable parity On/Off
  - Asynchronous (start-stop synchronized) or clock-synchronous communications selectable
  - Internal timer for dedicated baud rate (U-timer) on each channel
  - External clock can be used as transfer clock
  - Error detection function for parity, frame and overrun
- PPG : 16-bit × 6 ch
- Up/down counter : 2 ch (8-bit × 2 ch or 16-bit × 1 ch)
- Reload timer : 16-bit × 4 ch
- Free-run timer : 16-bit × 2 ch
- Watch timer : 15-bit × 1 ch
- PWC : 8-bit × 2 ch
- Input capture : 2 ch (interface with free-run timer 0)
- Output compare : 4 ch (free-run timer 0 and output compare unit 0/1 cooperate, free-run timer 1 and output compare units 2/3)
- LCD controller : SEG00 to SEG31/COM0 to COM3 (also serving as a port)
- Clock monitor (peripheral clock output function) : 1 ch
- Timebase/watchdog timer (26-bit)
- Real-time clock (counting even with the real-time clock stopped)
- Low Power Consumption Mode
- Sleep/stop function
- Package : LQFP-120, FLGA-128
- Technology : CMOS 0.35 µm
- Power supply
- Dual power supply configuration [internal logic 3.3 V, I/O 5.5 V(3.3 V for ADC and DAC input/output)]

Note : Do not set the external bus mode in which the MB91230 series cannot operate.

■ PIN ASSIGNMENT

• MB91233L, MB91F233, MB91F233L

(TOP VIEW)



* : Open-drain

(FPT-120P-M05)

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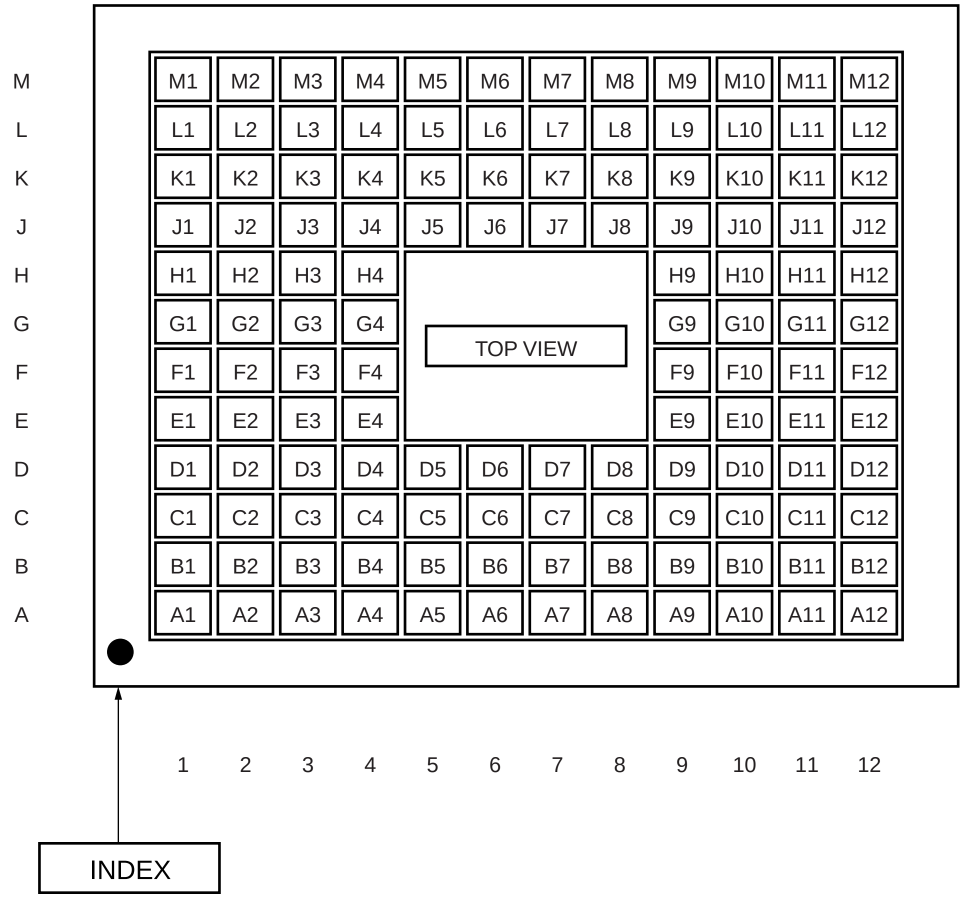
• MB91F233L



(LGA-128P-M01)

Pin correspondence table of LQFP-120 and FLGA-128 in MB91230 series (LGA-128P-M01)

LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name	LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name	LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name
1	A1	P26/SCK2	98	C9	P03/SIN1	18	G1	P42/PPG2
120	A2	P25/SOT2	93	C10	V2	15	G2	V_{CC}3B
117	A3	P22/PWI0/ OP2	85	C11	P72/COM2	*2	G3*4	V_{CC}3*4
114	A4	P17/INT7	87	C12	MD2	17	G4	V_{CC}3
—	A5	*5	10	D1	P37/ZIN1	71	G9	PA6/ SEG22
109	A6	P12/INT2	6	D2	P33/BIN0	75	G10	V_{CC}
107	A7	X1	8	D3	P35/AIN1	74	G11	PB1/ SEG25
103	A8	P10/INT0	119	D4	P24/SIN2	77	G12	PB2/ SEG26
100	A9	P05/SCK1	111	D5	P14/INT4	21	H1	P45/TOT1
97	A10	P02/SCK0	—	D6	*5	19	H2	P43/PPG3
94	A11	V3	101	D7	P06/IC0	23	H3	P47/CKOT
91	A12	V0	95	D8	P00/SIN0	20	H4	P44/TOT0
4	B1	P31/SCK3	89	D9	MD0	65	H9	PA0/ SEG16
118	B2	P23/PWI1/ OP3	86	D10	P73/COM3	72	H10	PA7/ SEG23
115	B3	P20/CKI0/ OP0	82	D11	P67/ SEG31*1	69	H11	PA4/ SEG20
112	B4	P15/INT5	84	D12	P71/COM1	73	H12	PB0/ SEG24
110	B5	P13/INT3	13	E1	X0A	24	J1	P50/INT8
106	B6	V_{SS}	9	E2	P36/BIN1	22	J2	P46/TOT2
104	B7	P11/INT1	12	E3	P41/PPG1	26	J3	P52/INT10
99	B8	P04/SOT1	5	E4	P32/AIN0	29	J4	P55/INT13/ TIN2
96	B9	P01/SOT0	81	E9	P66/ SEG30*1	35	J5	PD1/DA1
92	B10	V1	83	E10	P70/COM0	40	J6	PC1/AN1
88	B11	MD1	80	E11	P65/ SEG29*1	47	J7	V_{SS}
90	B12	$\overline{\text{INIT}}$	—	E12	*5	50	J8	P81/SEG1

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LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name	LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name	LQFP-120 No.	FLGA-128 No. (JEDEC No.)	Signal name
7	C1	P34/ZIN0	16	F1	V_{SS}	59	J9	P92/ SEG10
2	C2	P27/SIN3	—	F2	*5	68	J10	PA3/ SEG19
3	C3	P30/SOT3	14	F3	X1A	66	J11	PA1/ SEG17
116	C4	P21/CKI1/ OP1	11	F4	P40/PPG0	70	J12	PA5/ SEG21
113	C5	P16/INT6	78	F9	PB3/ SEG27	27	K1	P53/ INT11/ PPG4
108	C6	X0	79	F10	P64/ SEG28*1	25	K2	P51/INT9
105	C7	V_{CC}	76	F11	V_{SS}	33	K3	PF4/TIN3/ ADTG1
102	C8	P07/IC1	—	F12	*5	38	K4	AV_{SS}
41	K5	PC2/AN2	36	L4	AV_{CC}	37	M3	AVRH
44	K6	PC5/AN5	*3	L5*4	AVRL*4	39	M4	PC0/AN0
48	K7	V_{CC}3IO	43	L6	PC4/AN4	42	M5	PC3/AN3
53	K8	P84/SEG4	45	L7	PC6/AN6	46	M6	PC7/AN7
56	K9	P87/SEG7	49	L8	P80/SEG0	—	M7	*5
63	K10	P96/ SEG14	52	L9	P83/SEG3	51	M8	P82/SEG2
62	K11	P95/ SEG13	55	L10	P86/SEG6	54	M9	P85/SEG5
67	K12	PA2/ SEG18	58	L11	P91/SEG9	57	M10	P90/SEG8
30	L1	P56/ INT14/ TIN1	64	L12	P97/ SEG15	60	M11	P93/ SEG11
28	L2	P54/ INT12/ PPG5	31	M1	P57/ INT15/ TIN0/ ADTG0	61	M12	P94/ SEG12
32	L3	PF3/TOT3	34	M2	PD0/DA0			

*1 : Open-drain

*2 : Connected to pin 17(V_{CC}3) on the LQFP120 version

*3 : Connected to pin 38(AV_{SS}) on the LQFP120 version

*4 : Signals added to the FLGA version

*5 : NC pin on the FLGA version

■ PIN DESCRIPTION

Pin no. LQFP	Pin no. FLGA	Pin name	Circuit type	Description
1	A1	SCK2	D	UART2 clock input/output. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P26		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.
2	C2	SIN3	D	UART3 data input. When using this function, corresponding bit of DDR2 register is set to input.
		P27		General purpose input/output port. This function is always valid.
3	C3	SOT3	B	UART3 data output. This function is valid when corresponding bit of PFR3 register is set to peripheral function.
		P30		General purpose input/output port. This function is valid when corresponding bit of PFR3 register is set to port function.
4	B1	SCK3	B	UART3 clock input/output. This function is valid when corresponding bit of PFR3 register is set to peripheral function.
		P31		General purpose input/output port. This function is valid when corresponding bit of PFR3 register is set to port function.
5	E4	AIN0	B	Up/down counter 0 AIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P32		General purpose input/output port. This function is alwais valid.
6	D2	BIN0	B	Up/down counter 0 BIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P33		General purpose input/output port. This function is always valid.
7	C1	ZIN0	B	Up/down counter 0 ZIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P34		General purpose input/output port. This function is always valid.
8	D3	AIN1	B	Up/down counter 1 AIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P35		General purpose input/output port. This function is always valid.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
9	E2	BIN1	B	Up/down counter 1 BIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P36		General purpose input/output port. This function is always valid.
10	D1	ZIN1	B	Up/down counter 1 ZIN input. When using this function, corresponding bit of DDR3 register is set to input.
		P37		General purpose input/output port. This function is always valid.
11	F4	PPG0	D	PPG0 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P40		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
12	E3	PPG1	D	PPG1 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P41		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
13	E1	X0A	—	Sub-clock oscillation pin (32 kHz)
14	F3	X1A		
15	G2	V_{CC}3B	—	Power supply pin for backup (RTC)
16	F1	V_{SS}	—	Power supply pin (GND)
17	G4	V_{CC}3	—	Power supply pin (3.3 V internal logic)
18	G1	PPG2	D	PPG2 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P42		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
19	H2	PPG3	D	PPG3 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P43		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
20	H4	TOT0	D	Reload timer 0 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P44		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
21	H1	TOT1	D	Reload timer 1 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P45		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
22	J2	TOT2	D	Reload timer 2 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P46		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
23	H3	CKOT	D	Clock monitor function output pin. This function is valid when corresponding bit of PFR4 register is set to peripheral function.
		P47		General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function.
24	J1	INT8	C	External interrupt input. When using this function, corresponding bit of DDR5 register is set to input.
		P50		General purpose input/output port. This function is always valid.
25	K2	INT9	C	External interrupt input. When using this function, corresponding bit of DDR5 register is set to input.
		P51		General purpose input/output port. This function is always valid.
26	J3	INT10	C	External interrupt input. When using this function, corresponding bit of DDR5 register is set to input.
		P52		General purpose input/output port. This function is always valid.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
27	K1	PPG4	C	PPG4 output. This function is valid when corresponding bit of PFR5 register is set to peripheral function.
		INT11		External interrupt input. This function is enabled when corresponding bit of PFR5 register is set to port function and corresponding bit of DDR5 resister is set to input.
		P53		General purpose input/output port. This function is valid when corresponding bit of PFR5 register is set to port function.
28	L2	PPG5	C	PPG5 output. This function is valid when corresponding bit of PFR5 register is set to peripheral function.
		INT12		External interrupt input. This function is enabled when corresponding bit of PFR5 register is set to port function and corresponding bit of DDR5 resister is set to input.
		P54		General purpose input/output port. This function is valid when corresponding bit of PFR5 register is set to port function.
29	J4	TIN2	C	Reload timer 2 event input pin. This function is valid when corresponding bit of DDR5 register is set to input.
		INT13		External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input.
		P55		General purpose input/output port. This function is always valid.
30	L1	TIN1	C	Reload timer 1 event input pin. This function is valid when corresponding bit of DDR5 register is set to input.
		INT14		External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input.
		P56		General purpose input/output port. This function is always valid.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
31	M1	ADTG0	C	External trigger input pin of A/D converter 0. This function is valid when corresponding bit of DDR5 register is set to input.
		TIN0		Reload timer 0 event input pin. This function is valid when corresponding bit of DDR5 register is set to input.
		INT15		External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input.
		P57		General purpose input/output port. This function is always valid.
32	L3	TOT3	D	Reload timer 3 output port. This function is valid when corresponding bit of PFRF register is set to peripheral function.
		PF3		General purpose input/output port. This function is valid when corresponding bit of PFRF register is set to port function.
33	K3	ADTG1	D	External trigger input pin of A/D converter 1. This function is valid when corresponding bit of DDRF register is set to input.
		TIN3		Reload timer 3 event input pin. This function is valid when corresponding bit of DDRF register is set to input.
		PF4		General purpose input/output port. This function is always valid.
34	M2	DA0	F	D/A converter 0 output pin. This function is valid when corresponding bit of PFRD register is set to peripheral function.
		PD0		General purpose input/output port. This function is valid when corresponding bit of PFRD register is set to port function.
35	J5	DA1	F	D/A converter 1 output pin. This function is valid when corresponding bit of PFRD register is set to peripheral function.
		PD1		General purpose input/output port. This function is valid when corresponding bit of PFRD register is set to port function.
36	L4	AV_{CC}	—	Analog power supply (for A/D, D/A converter) .
37	M3	AVRH	—	Analog reference power supply (for A/D, D/A converter) .
38	K4	AV_{SS}	—	GND level input for analog circuit (for A/D, D/A converter) .

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
39 to 46	M4, J6, K5, M5, L6, K6, L7, M6	AN0 to AN7	E	Analog input pin for A/D converter. This function is valid when corresponding bit of PFRC register is set to peripheral function.
		PC0 to PC7		General purpose input/output port. This function is valid when corresponding bit of PFRC register is set to port function.
47	J7	V_{SS}	—	Power supply pin (GND)
48	K7	V_{CC}3IO	—	Power supply pin (analog-shared pin I/O)
49 to 56	L8, J8, M8, L9, K8, M9, L10, K9	SEG0 to SEG7	I	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR8 register is set to peripheral function.
		P80 to P87		General purpose input/output port. This function is valid when corresponding bit of PFR8 register is set to port function.
57 to 64	M10, L11, J9, M11, M12, K11, K10, L12	SEG8 to SEG15	I	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR9 register is set to peripheral function.
		P90 to P97		General purpose input/output port. This function is valid when corresponding bit of PFR9 register is set to port function.
65 to 72	H9, J11, K12, J10, H11, J12, G9, H10	SEG16 to SEG23	I	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRA register is set to peripheral function.
		PA0 to PA7		General purpose input/output port. This function is valid when corresponding bit of PFRA register is set to port function.
73, 74	H12, G11	SEG24, SEG25	I	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRB register is set to peripheral function.
		PB0, PB1		General purpose input/output port. This function is valid when corresponding bit of PFRB register is set to port function.
75	G10	V_{CC}	—	Power supply pin (5 V I/O MB91V230/F233)
				Power supply pin (3.3 V internal logic, I/O MB91F233L/MB91233L)
76	F11	V_{SS}	—	Power supply pin (GND)
77, 78	G12, F9	SEG26, SEG27	I	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRB register is set to peripheral function.
		PB2, PB3		General purpose input/output port. This function is valid when corresponding bit of PFRB register is set to port function.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
79 to 82	F10, E11, E9, D11	SEG28 to SEG31	J	LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR6 register is set to peripheral function.
		P64 to P67		General purpose input/output port. (open-drain) This function is valid when corresponding bit of PFR6 register is set to port function.
83 to 86	E10, D12, C11, D10	COM0 to COM3	I	LCD controller/driver common pins. This function is valid when corresponding bit of PFR7 register is set to peripheral function.
		P70 to P73		General purpose input/output port. This function is valid when corresponding bit of PFR7 register is set to port function.
87 to 89	C12, B11, D9	MOD2, MOD1, MOD0	H	Mode input pin.
90	B12	$\overline{\text{INIT}}$	G	External reset input.
91 to 94	A12, B10, C10, A11	V0 to V3	—	LCD controller/driver reference power supply input pins.
95	D8	SIN0	D	UART0 data input. When using this function, corresponding bit of DDR0 register is set to input.
		P00		General purpose input/output port. This function is always valid.
96	B9	SOT0	D	UART0 data output. This function is valid when corresponding bit of PFR0 register is set to peripheral function.
		P01		General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function.
97	A10	SCK0	D	UART0 clock input/output. This function is valid when corresponding bit of PFR0 register is set to peripheral function.
		P02		General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function.
98	C9	SIN1	D	UART1 data input. This function is valid when corresponding bit of DDR0 register is set to input.
		P03		General purpose input/output port. This function is always valid.

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Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
99	B8	SOT1	D	UART1 data output. This function is valid when corresponding bit of PFR0 register is set to peripheral function.
		P04		General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function.
100	A9	SCK1	D	UART1 clock input/output. This function is valid when corresponding bit of PFR0 register is set to peripheral function.
		P05		General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function.
101	D7	IC0	D	Input capture input 0. This function is valid when corresponding bit of DDR0 register is set to input.
		P06		General purpose input/output port. This function is always valid.
102	C8	IC1	D	Input capture input 1. This function is valid when corresponding bit of DDR0 register is set to input.
		P07		General purpose input/output port. This function is always valid.
103	A8	INT0	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P10		General purpose input/output port. This function is always valid.
104	B7	INT1	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P11		General purpose input/output port. This function is always valid.
105	C7	V_{CC}	—	Power supply pin (5 V I/O MB91V230/F233)
				Power supply pin (3.3 V internal logic, I/O MB91F233L/MB91233L)
106	B6	V_{SS}	—	Power supply pin (GND)
107	A7	X1	—	Main-clock oscillation pin
108	C6	X0	—	

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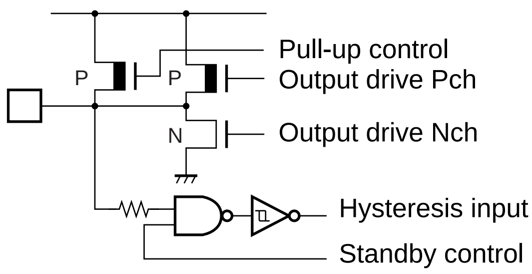
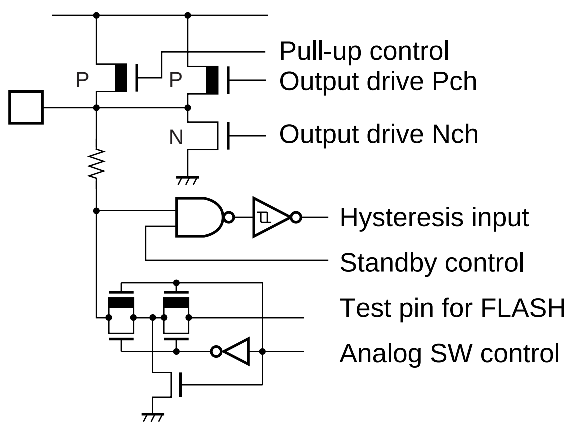
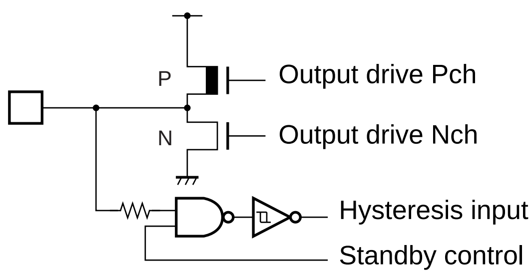
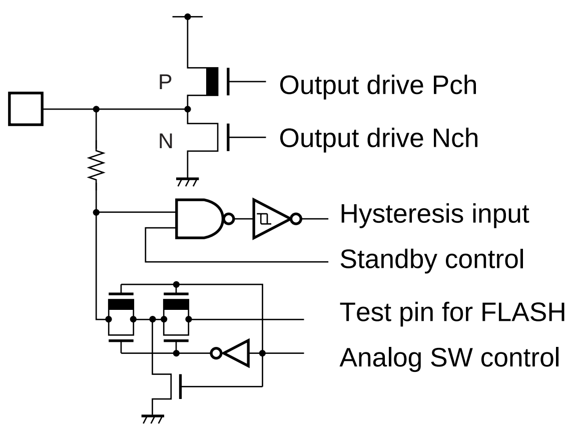
Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
109	A6	INT2	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P12		General purpose input/output port. This function is always valid.
110	B5	INT3	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P13		General purpose input/output port. This function is always valid.
111	D5	INT4	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P14		General purpose input/output port. This function is always valid.
112	B4	INT5	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P15		General purpose input/output port. This function is always valid.
113	C5	INT6	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P16		General purpose input/output port. This function is always valid.
114	A4	INT7	A	External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input.
		P17		General purpose input/output port. This function is always valid.
115	B3	CKI0	D	External clock input pin for free-run timer 0. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input.
		OP0		Output compare 0 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P20		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.

(Continued)

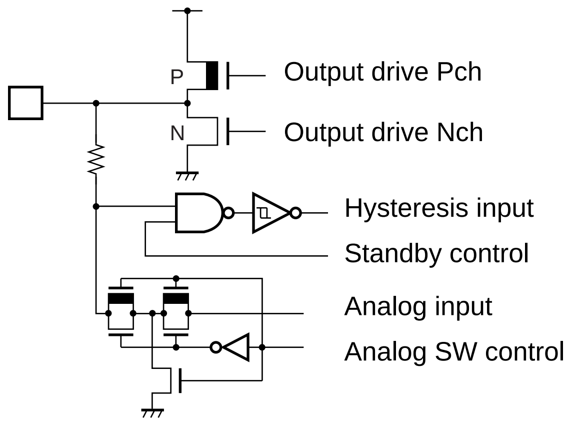
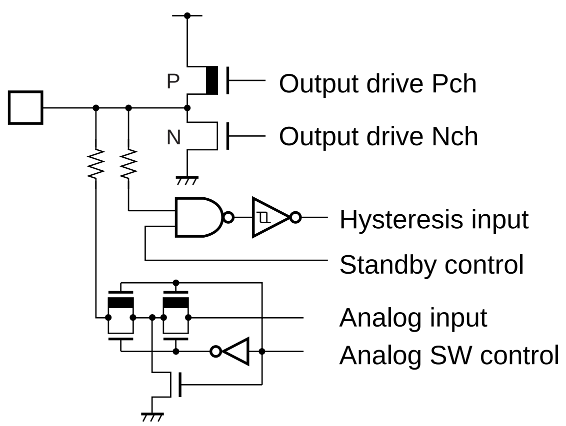
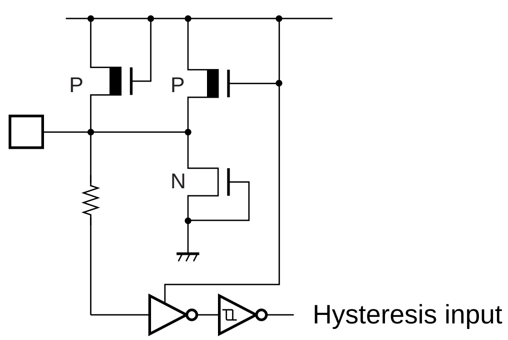
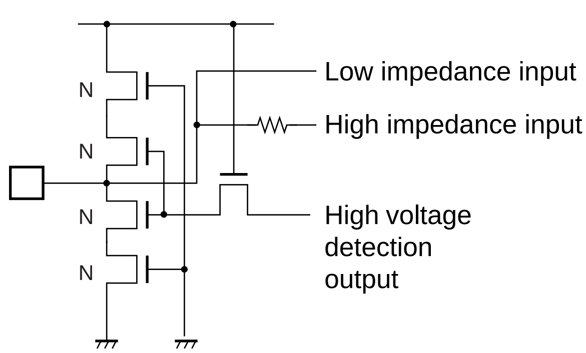
(Continued)

Pin no.		Pin name	Circuit type	Description
LQFP	FLGA			
116	C4	CKI1	D	External clock input pin for free-run timer 1. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input.
		OP1		Output compare1 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P21		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.
117	A3	PWI0	D	Pulse width counter 0 input. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input.
		OP2		Output compare2 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P22		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.
118	B2	PWI1	D	Pulse width counter 1 input. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input.
		OP3		Output compare3 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P23		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.
119	D4	SIN2	D	UART2 data input. This function is valid when corresponding bit of DDR2 register is set to input.
		P24		General purpose input/output port. This function is always valid.
120	A2	SOT2	D	UART2 data output. This function is valid when corresponding bit of PFR2 register is set to peripheral function.
		P25		General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function.
(38)	L5	AVRL	—	Analog reference power supply (for A/D converter)
—	A5, D6, E12, F2, F12, M7	NC	—	Unconnected pin.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		With Pull-up control (50 kΩ) CMOS level output I_{OH} = 4 mA/I_{OL} = 4 mA CMOS hysteresis input (with standby control)
B		With Pull-up control (50 kΩ) CMOS level output I_{OH} = 4 mA/I_{OL} = 4 mA CMOS hysteresis input (with standby control) Test pin for FLASH
C		CMOS level output CMOS hysteresis input (with standby control)
D		CMOS level output I_{OH} = 4 mA/I_{OL} = 4 mA CMOS hysteresis input (with standby control) Test pin for FLASH

(Continued)

Type	Circuit type	Remarks
E		CMOS level output I_{OH} = 4 mA/I_{OL} = 4 mA CMOS hysteresis input (with standby control) Also serving as an analog input
F		CMOS level output I_{OH} = 4 mA/I_{OL} = 4 mA CMOS hysteresis input (with standby control) Also serving as an analog input
G		With Pull-up control (50 kΩ) CMOS hysteresis input
H		High withstand-voltage input CMOS input (hysteresis level)

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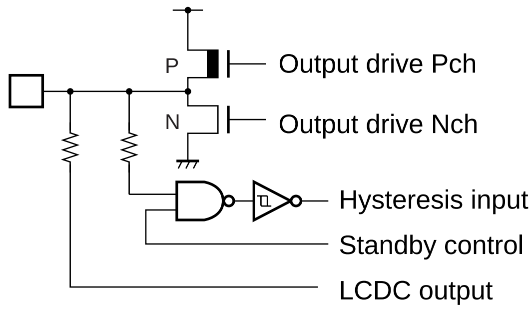
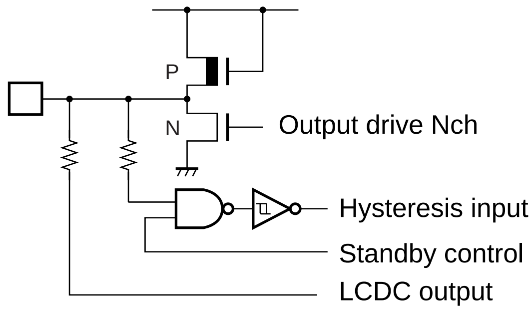
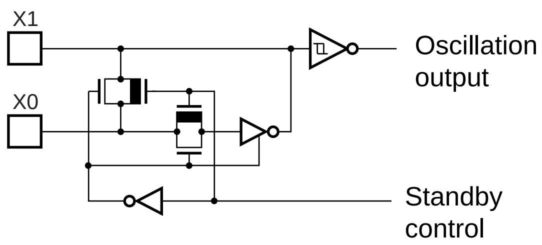
Type	Circuit type	Remarks
I		CMOS level output $I_{OH} = 4$ mA/$I_{OL} = 4$ mA CMOS hysteresis input (with standby control) LCDC output
J		CMOS level output (open-drain) $I_{OL} = 20$ mA CMOS hysteresis input (with standby control) LCDC output
K		Oscillation circuit

■ HANDLING DEVICES

Preventing Latchup

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} and V_{SS}.

A latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the absolute maximum rating.

Treatment of Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

About Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

About Crystal Oscillator Circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

Treatment of NC and OPEN Pins

Pins marked as NC and OPEN must be left open-circuit.

About Mode Pins (MD0 to MD2)

These pins should be connected directly to V_{CC} or V_{SS}.

To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

Operation at Start-up

Be sure to execute setting initialized reset (INIT) with $\overline{\text{INIT}}$ pin immediately after start-up.

Also, in order to provide the oscillation stabilization wait time for the oscillation circuit immediately after start-up, hold the “L” level input to the $\overline{\text{INIT}}$ pin for the required stabilization wait time. (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value) .

About Oscillation Input at Power On

When turning the power on, maintain clock input untill the device is released from the oscillation stabilization wait state.

Clock Control Block

Input the “L” signal to the $\overline{\text{INIT}}$ pin to assure the clock oscillation stabilization wait time.

Switch Shared Port Function

To switch between the use as a port and the use as a dedicated pin, use the port function register (PFR) .

Low Power Consumption Mode

To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR : timebse counter control register) and be sure to use the following sequence

```
 (LDI     #value_of_standby, R0)   : value_of_standby is write data to STCR.
 (LDI     #_STCR, R12)             : _STCR is address (481H) of STCR.
 STB      R0, @R12                 : Writing to standby control register (STCR)
 LDUB     @R12, R0                 : STCR read for synchronous standby
 LDUB     @R12, R0                 : Dummy re-read of STCR
 NOP                               : NOP × 5 for arrangement of timing
 NOP
 NOP
 NOP
 NOP
```

In addition, please set I flag, ILM, and ICR to diverge to the interruption handler that is the return factor after the standby returns.

- Please do not do the following when the monitor debugger is used.
- Break point setting for above instruction lines
- Step execution for above instruction lines

Power-on sequence for dual-power-supply model

- Notes on the power-on and power-off sequences
  Power-on sequence : Vcc3B, Vcc3→Vcc→Vcc3IO, AVRH, V0-V3
  Power-off sequence : Vcc3IO, AVRH, V0-V3 Vcc3→Vcc→Vcc3B, Vcc3
  When V_{CC} is turned on earlier, a potential difference between V_{CC} and $V_{CC}3$ must fall within 3.6 V.
- The LCD power supply V3 must not exceed V_{CC} in voltage. Apply V3 after turning on $V_{CC}3$.
- Turn on $V_{CC}3$ before applying the analog power supply AV_{CC} or an analog signal.

Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) acceptance of a user interrupt, (b) single-stepped, or (c) breaks in response to a data event or emulator menu :

  1) The D0 and D1 flags are updated in advance.

  2) An EIT handling routine (user interrupt or emulator) is executed.

  3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed, and the D0 and D1 flags are updated to the same values as in 1).

- The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed to allow the interrupt.

  1) The PS register is updated in advance.

  2) An EIT handling routine (user interrupt) is executed.

  3) Upon returning from the EIT, the above instructions are executed, and the PS register is updated to the same value as in 1).

Watchdog Timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, see the function description of watchdog timer.

Step execution of RETI instruction

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution. This will prevent the main routine and low-interrupt-level programs from being executed.

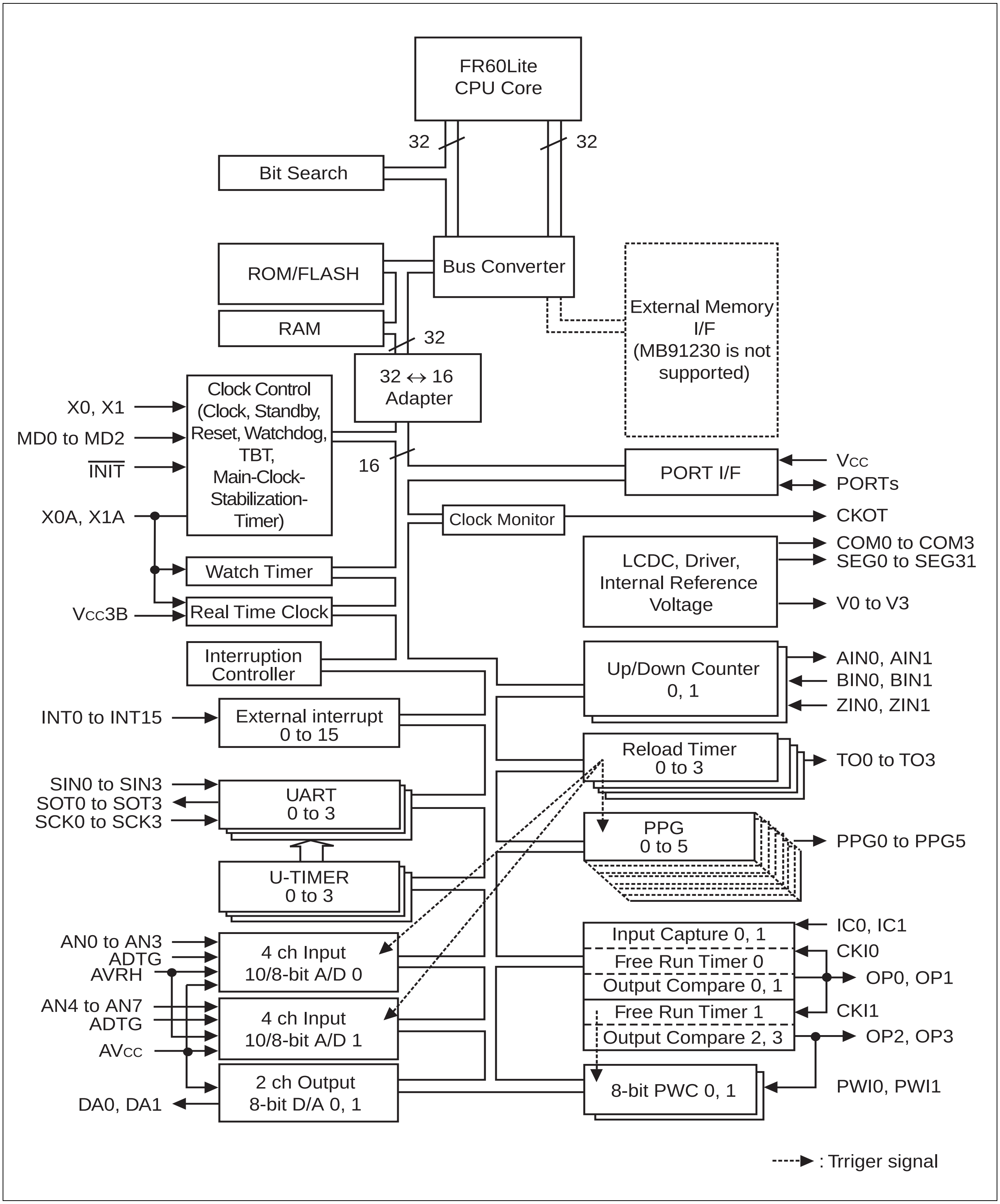
Do not execute step of RETI instruction for escape.

Disable the corresponding interrupt and execute debugger when the corresponding interrupt routine no longer needs debugging.

Operand Break

Do not apply a data event break to access to the area containing the address of a system stack pointer.

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory space

The FR60 Lite family has 4 gigabytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct Addressing Areas

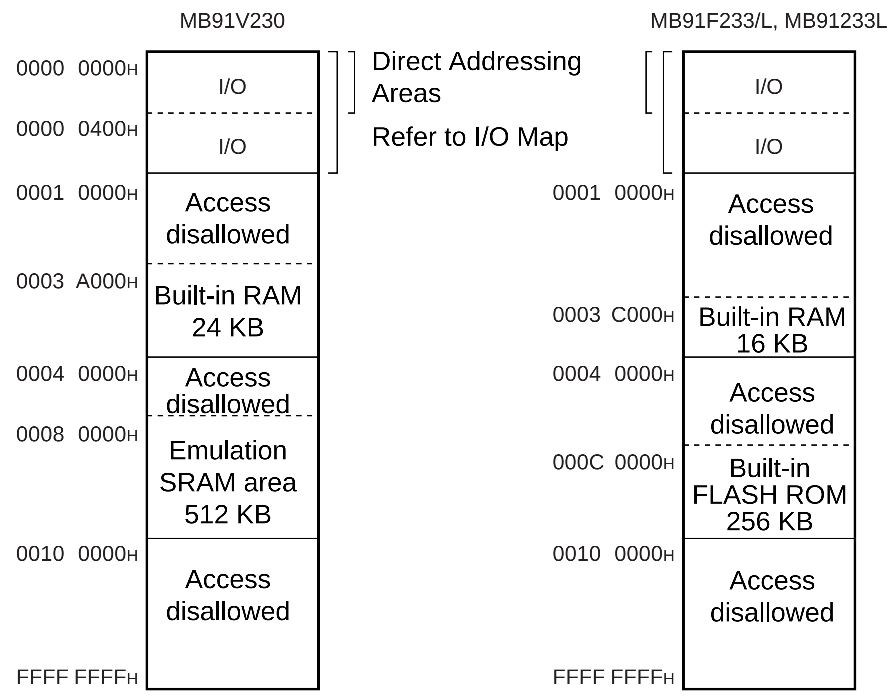
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The size of directly addressable areas depends on the length of the data being accessed as shown below.

- byte data access : 0 to $0FF_H$
- half word data access : 0 to $1FF_H$
- word data access : 0 to $3FF_H$

2. Memory Map



Note : Do not set the external bus mode in which the MB91230 series cannot operate.

■ MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and a mode data to set the operation mode.

- Mode Pins

The MD2, MD1, and MD0 pins specify how the mode vector fetch and reset vector fetch is performed.

Setting is prohibited other than that shown in the following table.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	Not supported by this model.

- Mode data

Data written to the internal mode register (MODR) by a mode vector fetch is called mode data.

After an operation mode has been set in the mode register, the device operates in the operation mode.

The mode data is set by all reset source. User programs cannot set data to the mode register.

Details of mode data description

bit	31	30	29	28	27	26	25	24
	0	0	0	0	0	1	1	1

Operation mode setting bits

[bit31 to bit24] Reserved bit

Be sure to set this bit to “00000111”.
Operation is not guaranteed when any value other than “00000111” is set.

Note : Mode data set in the mode vector must be placed as byte data at 0x000FFFF8H.
Use the highest byte from bit31 to bit24 for placement as the FR family uses the big endian for byte endian.

		bit 31 - 24	23 - 16	15 - 8	7 - 0
Incorrect	0x000FFFF8H	XXXXXXXX	XXXXXXXX	XXXXXXXX	Mode Data
Correct	0x000FFFF8H	Mode Data	XXXXXXXX	XXXXXXXX	XXXXXXXX
	0x000FFFFCH	Reset Vector			

■ I/O Map

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port data register

Read/write attribute Access unit
(B : byte, H : half word, W : word)

Initial value of register after reset

Register name (column 1 of the register is at address 4n, column 2 is at address 4n + 1...)

Leftmost register address (For word-length access, column 1 of the register becomes the MSB of the data.)

Note : Initial values of register bits are represented as follows :
- " 1 " : Initial Value " 1 "
- " 0 " : Initial Value " 0 "
- " X " : Initial Value " undefined"
- " - " : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	Port data register
000004H	PDR4 [R/W] B XXXXXXXX	PDR5 [R/W] B XXXXXXXX	PDR6 [R/W] B XXXX----	PDR7 [R/W] B ----XXXX	
000008H	PDR8 [R/W] B XXXXXXXX	PDR9 [R/W] B XXXXXXXX	PDRA [R/W] B XXXXXXXX	PDRB [R/W] B ----XXXX	
00000CH	PDRC [R/W] B XXXXXXXX	PDRD [R/W] B ------XX	—	PDRF [R/W] ---XX---	
000010H to 00003CH	—	—	—	—	Unused
000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to 7)
000044H	DICR [R/W] B, H, W -------0	—	—		Delay interrupt
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	—		TMCSR0 [R/W] B, H, W ----0000 00000000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054H	—		TMCSR1 [R/W] B, H, W ----0000 00000000		
000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	—		TMCSR2 [R/W] B, H, W ----0000 00000000		
000060H	SSR0 [R/W] B, H, W 00001000	SIDR0 [R] B, H, W SODR0 [W] B, H, W XXXXXXXX	SCR0 [R/W] B, H, W 00000100	SMR0 [R/W] B, H, W 00--0-0-	UART0
000064H	UTIM0 [R] H (UTIMR0 [W] H) 00000000 00000000		—	UTIMC0 [R/W] B 0--00001	U-TIMER0
000068H	SSR1 [R/W] B, H, W 00001000	SIDR1 [R] B, H, W SODR1 [W] B, H, W XXXXXXXX	SCR1 [R/W] B, H, W 00000100	SMR1 [R/W] B, H, W 00--0-0-	UART1
00006CH	UTIM1 [R] H (UTIMR1 [W] H) 00000000 00000000		—	UTIMC1 [R/W] B 0--00001	U-TIMER1

(Continued)

Address	Register +0	Register +1	Register +2	Register +3	Block
000070H	SSR2 [R/W] B, H, W 00001000	SIDR2 [R] B, H, W SODR2 [W] B, H, W XXXXXXXX	SCR2 [R/W] B, H, W 00000100	SMR2 [R/W] B, H, W 00--0-0-	UART2
000074H	UTIM2 [R] H (UTIMR1 [W] H) 00000000 00000000		—	UTIMC2 [R/W] B 0--00001	U-TIMER2
000078H	ADCS0 [R/W] H, W XXXXXXXX XXXXXXXX		ADCT0 [R/W] H, W 000-0000 -000--00		A/D converter 0 (series-parallel type)
00007CH	ADT00 (ADTH0/ADTL0) [R] H, W 000000XX XXXXXXXX		ADT01 (ADTH1/ADTL1) [R] H, W 000000XX XXXXXXXX		
000080H	ADT02 (ADTH2/ADTL2) [R] H, W 000000XX XXXXXXXX		ADT03 (ADTH3/ADTL3) [R] H, W 000000XX XXXXXXXX		
000084H	ADCS1 [R/W] H, W XXXXXXXX XXXXXXXX		ADCT1 [R/W] H, W 000-0000 --000--00		A/D converter 1 (series-parallel type)
000088H	ADT10 (ADTH0/ADTL0) [R] H, W 000000XX XXXXXXXX		ADT11 (ADTH1/ADTL1) [R] H, W 000000XX XXXXXXXX		
00008CH	ADT12 (ADTH2/ADTL2) [R] H, W 000000XX XXXXXXXX		ADT13 (ADTH3/ADTL3) [R] H, W 000000XX XXXXXXXX		
000090H	—	—	DACR1 [R/W] B, H, W -------0	DACR0 [R/W] B, H, W -------0	D/A converter
000094H	—	—	DADR1 [R/W] B, H, W XXXXXXXX	DADR0 [R/W] B, H, W XXXXXXXX	
000098H	LCDCMR [R/W] B, H, W ----0000	—	LCR0 [R/W] B, H, W 00010000	LCR1 [R/W] B, H, W 00000000	LCD controller/driver
00009CH	VRAM0 [R/W] B, H, W XXXXXXXX	VRAM1 [R/W] B, H, W XXXXXXXX	VRAM2 [R/W] B, H, W XXXXXXXX	VRAM3 [R/W] B, H, W XXXXXXXX	
0000A0H	VRAM4 [R/W] B, H, W XXXXXXXX	VRAM5 [R/W] B, H, W XXXXXXXX	VRAM6 [R/W] B, H, W XXXXXXXX	VRAM7 [R/W] B, H, W XXXXXXXX	
0000A4H	VRAM8 [R/W] B, H, W XXXXXXXX	VRAM9 [R/W] B, H, W XXXXXXXX	VRAM10 [R/W] B, H, W XXXXXXXX	VRAM11 [R/W] B, H, W XXXXXXXX	
0000A8H	VRAM12 [R/W] B, H, W XXXXXXXX	VRAM13 [R/W] B, H, W XXXXXXXX	VRAM14 [R/W] B, H, W XXXXXXXX	VRAM15 [R/W] B, H, W XXXXXXXX	
0000ACH	CKR [R/W] B, H, W ----0000	—	—	—	Clock monitor

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000B0H	RCR1 [W] B, H, W 00000000	RCR0 [W] B, H, W 00000000	UDCR1 [R] B, H, W 00000000	UDCR0 [R] B, H, W 00000000	Up/down counter0, 1
0000B4H	CCRH0 [R/W] B, H, W 00000000	CCRL0 [R/W] B, H, W 00001000	—	CSR0 [R/W] B, H, W 00000000	
0000B8H	CCRH1 [R/W] B, H, W 00000000	CCRL1 [R/W] B, H, W 00001000	—	CSR1 [R/W] B, H, W 00000000	
0000BCH	—	—	—	—	unused
0000C0H	SSR [R/W] B, H, W 00001000	SIDR 3 [R] B, H, W SODR 3 [W] B, H, W XXXXXXXX	SCR [R/W] B, H, W 00000100	SMR [R/W] B, H, W 00--0-0-	UART3
0000C4H	UTIM [R] H (UTIMR [W] H) 00000000 00000000		—	UTIMC [R/W] B 0--00001	U-TIMER3
0000C8H	TMRLR3 [W] H, W XXXXXXXX XXXXXXXX		TMR3 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 3
0000CCH	—		TMCSR3 [R/W] B, H, W ---00000 00000000		
0000D0H	EIRR1 [R/W] B, H, W 00000000	ENIR1 [R/W] B, H, W 00000000	ELVR1 [R/W] B, H, W 00000000 00000000		External interrupt (INT8 to 16)
0000D4H	TCDT0 [R/W] H, W 00000000 00000000		—	TCCS0 [R/W] B, H, W 00000000	Free-run timer 0
0000D8H	TCDT1 [R/W] H, W 00000000 00000000		—	TCCS1 [R/W] B, H, W 00000000	Free-run timer 1
0000DCH	IPCP1 [R] H, W XXXXXXXX XXXXXXXX		IPCP0 [R] H, W XXXXXXXX XXXXXXXX		Input capture
0000E0H	—	—	—	ICS01 [R/W] B, H, W 00000000	
0000E4H	OCCP1 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP0 [R/W] H, W XXXXXXXX XXXXXXXX		Output compare
0000E8H	OCCP3 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP2 [R/W] H, W XXXXXXXX XXXXXXXX		
0000ECH	OCS23 [R/W] B, H, W ---0--00 0000--00		OCS01 [R/W] B, H, W ---0-00 0000--00		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000F0H	PWCC0 [R/W] B, H, W 0---00-0	PWCD0 [R] B, H, W XXXXXXXX	PWCC1 [R/W] B, H, W 0---00-0	PWCD1 [R] B, H, W XXXXXXXX	PWC0, 1
0000F4H	—	WTDBL [R/W] B -------0	WTCR [R/W] B, H 00000000 000-00-X		Real-time clock
0000F8H	—	WTBR0 [R/W] B ---XXXXX	WTBR1 [R/W] B XXXXXXXX	WTBR2 [R/W] B XXXXXXXX	
0000FCH	WTHR [R/W] B, H ---XXXXX	WTMR [R/W] B, H --XXXXXX	WTSR [R/W] B --XXXXXX	—	
000100H to 000114H	—	—	—	—	Unused
000118H	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B 00000000	PPG
00011CH	—		—		Unused
000120H	PTMR0 [R] H, W 11111111 11111111		PCSR0 [W] H, W XXXXXXXX XXXXXXXX		PPG0
000124H	PDUT0 [W] H, W XXXXXXXX XXXXXXXX		PCNH0 [R/W] B, H, W 00000000	PCNL0 [R/W] B, H, W 00000000	
000128H	PTMR1 [R] H, W 11111111 11111111		PCSR1 [W] H, W XXXXXXXX XXXXXXXX		PPG1
00012CH	PDUT1 [W] H, W XXXXXXXX XXXXXXXX		PCNH1 [R/W] B, H, W 00000000	PCNL1 [R/W] B, H, W 00000000	
000130H	PTMR2 [R] H, W 11111111 11111111		PCSR2 [W] H, W XXXXXXXX XXXXXXXX		PPG2
000134H	PDUT2 [W] H, W XXXXXXXX XXXXXXXX		PCNH2 [R/W] B, H, W 00000000	PCNL2 [R/W] B, H, W 00000000	
000138H	PTMR3 [R] H, W 11111111 11111111		PCSR3 [W] H, W XXXXXXXX XXXXXXXX		PPG3
00013CH	PDUT3 [W] H, W XXXXXXXX XXXXXXXX		PCNH3 [R/W] B, H, W 00000000	PCNL3 [R/W] B, H, W 00000000	
000140H	PTMR4 [R] H, W 11111111 11111111		PCSR4 [W] H, W XXXXXXXX XXXXXXXX		PPG4
000144H	PDUT4 [W] H, W XXXXXXXX XXXXXXXX		PCNH4 [R/W] B, H, W 00000000	PCNL4 [R/W] B, H, W 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000148H	PTMR5 [R] H, W 11111111 11111111		PCSR5 [W] H, W XXXXXXXX XXXXXXXX		PPG5
00014CH	PDUT5 [W] H, W XXXXXXXX XXXXXXXX		PCNH5 [R/W] B, H, W 00000000	PCNL5 [R/W] B, H, W 00000000	
000150H to 0001FCH	—	—	—	—	Unused
000200H to 0003ECH	—	—	—	—	Unused
0003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search
0003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] B 00000000	DDR1 [R/W] B 00000000	DDR2 [R/W] B 00000000	DDR3 [R/W] B00000000	Data direction register
000404H	DDR4 [R/W] B 00000000	DDR5 [R/W] B 00000000	DDR6 [R/W] B 0000----	DDR7 [R/W] B ----0000	
000408H	DDR8 [R/W] B 00000000	DDR9 [R/W] B 00000000	DDRA [R/W] B 00000000	DDRB [R/W] B ----0000	
00040CH	DDRC [R/W] B 00000000	DDRD [R/W] B ------00	—	DDRF [R/W] B ---00---	
000410H to 00041CH	—	—	—	—	Unused
000420H	PFR0 [R/W] B --00-00-	PFR1 [R/W] B --------	PFR2 [R/W] B -00-0000	PFR3 [R/W] B ------00	Port function register
000424H	PFR4 [R/W] B 00000000	PFR5 [R/W] B ---00---	PFR6 [R/W] B 0000----	PFR7 [R/W] B ----0000	
000428H	PFR8 [R/W] B 00000000	PFR9 [R/W] B 00000000	PFRA [R/W] B 00000000	PFRB [R/W] B ----0000	
00042CH	PFRC [R/W] B --------	PFRD [R/W] B ------00	—	PFRF [R/W] B ----0---	
000430H to 00043CH	—	—	—	—	Unused

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt control unit
000444H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
00044CH	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
00045CH	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
00046CH	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470H to 00047CH	—	—	—	—	Unused

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000480H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXXX00	CTBR [W] B, H, W XXXXXXXX	Clock control
000484H	CLKR [R/W] B, H, W 00000000	WPR [R/W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488H	—	—	OSCCR [R/W] B XXXXXXX0	—	
00048CH	WPCR [R/W] B 00---000	—	—	—	Watch timer
000490H	OSCR [R/W] B 00---000	—	—	—	Main clock oscillation stabilization wait timer
000494H to 0004FCH	—	—	—	—	Unused
000500H	—	PCR1 [R/W] B 00000000	—	PCR3 [R/W] B 00000000	Pull-up control register
000504H to 00051CH	—	—	—	—	Unused
000520H to 0007F8H	—	—	—	—	Unused
0007FCH	—	MODR* XXXXXXXX	—	—	Operation mode
000800H to 000AFCH	—	—	—	—	Unused
000B00H to 000FFCH	—	—	—	—	Unused
001000H to 001FFCH	—	—	—	—	Unused

* : This register is set when the mode vector is fetched. Not user-accessible.

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	10	16			
Reset	0	00	—	3FCH	000FFFFCH
Mode vector	1	01	—	3F8H	000FFFF8H
System reserved	2	02	—	3F4H	000FFFF4H
System reserved	3	03	—	3F0H	000FFFF0H
System reserved	4	04	—	3ECH	000FFFECH
System reserved	5	05	—	3E8H	000FFFE8H
System reserved	6	06	—	3E4H	000FFFE4H
Coprocessor absent trap	7	07	—	3E0H	000FFFE0H
Coprocessor error trap	8	08	—	3DCH	000FFFDCH
INTE instruction	9	09	—	3D8H	000FFFD8H
Instruction break exception	10	0A	—	3D4H	000FFFD4H
Operand break trap	11	0B	—	3C0H	000FFFD0H
Step trace trap	12	0C	—	3CCH	000FFFCCH
NMI request (tool)	13	0D	—	3C8H	000FFFC8H
Undefined instruction exception	14	0E	—	3C4H	000FFFC4H
NMI request (This model has no NMI request)	15	0F	15 (FH) fixed	3C0H	000FFFC0H
External interrupt 0	16	10	ICR00	3BCH	000FFFBCH
External interrupt 1	17	11	ICR01	3B8H	000FFFB8H
External interrupt 2	18	12	ICR02	3B4H	000FFFB4H
External interrupt 3	19	13	ICR03	3B0H	000FFFB0H
External interrupt 4	20	14	ICR04	3ACH	000FFFACH
External interrupt 5	21	15	ICR05	3A8H	000FFFA8H
External interrupt 6	22	16	ICR06	3A4H	000FFFA4H
External interrupt 7	23	17	ICR07	3A0H	000FFFA0H
Reload timer 0	24	18	ICR08	39CH	000FFF9CH
Reload timer 1	25	19	ICR09	398H	000FFF98H
Reload timer 2	26	1A	ICR10	394H	000FFF94H
UART0(Reception completed)	27	1B	ICR11	390H	000FFF90H
UART0 (Transmission completed)	28	1C	ICR12	38CH	000FFF8CH
UART1 (Reception completed)	29	1D	ICR13	388H	000FFF88H
UART1 (Transmission completed)	30	1E	ICR14	384H	000FFF84H
UART2 (Reception completed)	31	1F	ICR15	380H	000FFF80H
UART2 (Transmission completed)	32	20	ICR16	37CH	000FFF7CH

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	10	16			
UART3 (Reception completed)	33	21	ICR17	378H	000FFF78H
UART3 (Transmission completed)	34	22	ICR18	374H	000FFF74H
A/D ch0	35	23	ICR19	370H	000FFF70H
A/D ch1	36	24	ICR20	36CH	000FFF6CH
External interrupt8	37	25	ICR21	368H	000FFF68H
External interrupt9	38	26	ICR22	364H	000FFF64H
External interrupt 10	39	27	ICR23	360H	000FFF60H
External interrupt 11	40	28	ICR24	35CH	000FFF5CH
External interrupt 12	41	29	ICR25	358H	000FFF58H
External interrupt 13	42	2A	ICR26	354H	000FFF54H
External interrupt 14	43	2B	ICR27	350H	000FFF50H
External interrupt 15	44	2C	ICR28	34CH	000FFF4CH
Real-time clock	45	2D	ICR29	348H	000FFF48H
Main clock oscillation stabilization wait timer	46	2E	ICR30	344H	000FFF44H
Timebase timer 0 overflow	47	2F	ICR31	340H	000FFF40H
Reload timer 3	48	30	ICR32	33CH	000FFF3CH
Watch timer	49	31	ICR33	338H	000FFF38H
UD Counter 0	50	32	ICR34	334H	000FFF34H
UD Counter 1	51	33	ICR35	330H	000FFF30H
PPG 0/1	52	34	ICR36	32CH	000FFF2CH
PPG 2/3	53	35	ICR37	328H	000FFF28H
PPG 4/5	54	36	ICR38	324H	000FFF24H
Free-run timer 0	55	37	ICR39	320H	000FFF20H
Free-run timer 1	56	38	ICR40	31CH	000FFF1CH
ICU 0 (capture)	57	39	ICR41	318H	000FFF18H
ICU 1 (capture)	58	3A	ICR42	314H	000FFF14H
OCU 0 (match)	59	3B	ICR43	310H	000FFF10H
OCU 1 (match)	60	3C	ICR44	30CH	000FFF0CH
OCU 2 (match)	61	3D	ICR45	308H	000FFF08H
OCU 3 (match)	62	3E	ICR46	304H	000FFF04H
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H
System reserved	66	42	—	2F4H	000FFEF4H

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	10	16			
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$
System reserved	73	49	—	$2D8_H$	$000FFED8_H$
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
  Indicates that the input function can be used.

- Input 0 fixed
  Indicates that the input level has been internally fixed to be “0” to prevent leakage when the input is released.

- Output Hi-Z
  Means the placing of a pin in a high impedance state by preventing the transistor for driving the pin from driving.

- Output is maintained
  Indicates the output in the output state existing immediately before this mode is established. If the device enters this mode with an internal output peripheral operating or while serving as an output port, the output is performed by the internal peripheral or the port output is maintained, respectively.

- State existing immediately before is maintained
  When the device serves for output or input immediately before entering this mode, the device maintains the output or is ready for the input, respectively.

• Pin Status List

Pin no.	Pin name	Port name	Specified function name			At initializing		At sleep mode	At Stop mode		Remarks
			Input	Output	Input/ Output	Function name	Reset initialization		HIZ = 0	HIZ = 1	
1	P26/ SCK2	P26	—	—	SCK2	P26	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
2	P27/ SIN3	P27	SIN3	—	—	P27					
3	P30/ SOT3	P30	—	SOT3	—	P30					Pull-up options can be selected
4	P31/ SCK3	P31	—	—	SCK3	P31					Pull-up options can be selected
5	P32/ AIN0	P32	AIN0	—	—	P32					Pull-up options can be selected
6	P33/ BIN0	P33	BIN0	—	—	P33					Pull-up options can be selected
7	P34/ ZIN0	P34	ZIN0	—	—	P34					Pull-up options can be selected
8	P35/ AIN1	P35	AIN1	—	—	P35					Pull-up options can be selected
9	P36/ BIN1	P36	BIN1	—	—	P36					Pull-up options can be selected
10	P37/ ZIN1	P37	ZIN1	—	—	P37					Pull-up options can be selected
11	P40/ PPG0	P40	—	PPG 0	—	P40					
12	P41/ PPG1	P41	—	PPG 1	—	P41					

(Continued)

Pin no.	Pin name	Port name	Specified function name: Input	Specified function name: Output	Specified function name: Input/Output	At initializing: Function name	At initializing: Reset initialization	At sleep mode	At Stop mode: HIZ = 0	At Stop mode: HIZ = 1	Remarks
13	X0A	—	—	—	—	—	—	—	—	—	
14	X1A	—	—	—	—	—	—	—	—	—	
15	V_{CC}3B/ V_{CC}	—	—	—	—	—	—	—	—	—	
16	V_{SS}	—	—	—	—	—	—	—	—	—	
17	V_{CC}3	—	—	—	—	—	—	—	—	—	
18	P42/ PPG2	P42	—	PPG2	—	P42	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
19	P43/ PPG3	P43	—	PPG3	—	P43					
20	P44/ TOT0	P44	—	TOT0	—	P44					
21	P45/ TOT1	P45	—	TOT1	—	P45					
22	P46/ TOT2	P46	—	TOT2	—	P46					
23	P47/ CKOT	P47	—	CKOT	—	P47					
24	P50/ INT8	P50	INT8	—	—	P50			P : Retention of the immediately prior state F : Input enabled	P : Output Hi-Z F : Input enabled	
25	P51/ INT9	P51	INT9	—	—	P51					
26	P52/ INT10	P52	INT10	—	—	P52					
27	P53/ INT11/ PPG4	P53	INT11	PPG4	—	P53					
28	P54/ INT12/ PPG5	P54	INT12	PPG5	—	P54					
29	P55/ INT13/ TIN2	P55	INT13 TIN2	—	—	P55					
30	P56/ INT14/ TIN1	P56	INT14 TIN1	—	—	P56					

Note : P : Port selected, F : Specified function selected

(Continued)

Pin no.	Pin name	Port name	Specified function name			At initializing		At sleep mode	At Stop mode		Re-marks
			Input	Output	Input/ Output	Function name	Reset initialization		HIZ = 0	HIZ = 1	
31	P57/ INT15/ TIN0/ ADTG0	P57	INT15 TIN0 ADTG0	—	—	P57	Output Hi-Z/ Input enabled	Retention of the immediately prior state	P : Retention of the immediately prior state F : Input enabled	P : Output Hi-Z F : Input 0 enabled	
32	PF3/ TOT3	PF3	—	TOT3	—	PF3			Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
33	PF4/ TIN3/ ADTG1	PF4	TIN3 ADTG1	—	—	PF4					
34	PD0/ DA0	PD0	—	DA0	—	PD0					
35	PD1/ DA1	PD1	—	DA1	—	PD1					
36	AVcc	—	—	—	—	—	—	—	—	—	
37	AVRH	—	—	—	—	—	—	—	—	—	
38	AVss	—	—	—	—	—	—	—	—	—	
39	PC0/ AN0	PC0	AN0	—	—	PC0	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
40	PC1/ AN1	PC1	AN1	—	—	PC1					
41	PC2/ AN2	PC2	AN2	—	—	PC2	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
42	PC3/ AN3	PC3	AN3	—	—	PC3					
43	PC4/ AN4	PC4	AN4	—	—	PC4					
44	PC5/ AN5	PC5	AN5	—	—	PC5					
45	PC6/ AN6	PC6	AN6	—	—	PC6					
46	PC7/ AN7	PC7	AN7	—	—	PC7					

Note : P : Port selected, F : Specified function selected

(Continued)

<table>
<tr><th rowspan="2">Pin no.</th><th rowspan="2">Pin name</th><th rowspan="2">Port name</th><th colspan="3">Specified function name</th><th colspan="2">At initializing</th><th rowspan="2">At sleep mode</th><th colspan="2">At Stop mode</th><th rowspan="2">Re-marks</th></tr>
<tr><th>Input</th><th>Output</th><th>Input/ Output</th><th>Function name</th><th>Reset initialization</th><th>HIZ = 0</th><th>HIZ = 1</th></tr>
<tr><td>47</td><td>V_{SS}</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>48</td><td>V_{CC}3IO</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>49</td><td>P80/ SEG0</td><td>P80</td><td>—</td><td>SEG0</td><td>—</td><td>P80</td><td rowspan="15">Output Hi-Z/ Input enabled</td><td rowspan="15">Retention of the immediately prior state</td><td rowspan="15">Retention of the immediately prior state</td><td rowspan="15">P : Output Hi-Z/ Input 0 fixed
F : Retention of the immediately prior state</td><td></td></tr>
<tr><td>50</td><td>P81/ SEG1</td><td>P81</td><td>—</td><td>SEG1</td><td>—</td><td>P81</td><td></td></tr>
<tr><td>51</td><td>P82/ SEG2</td><td>P82</td><td>—</td><td>SEG2</td><td>—</td><td>P82</td><td></td></tr>
<tr><td>52</td><td>P83/ SEG3</td><td>P83</td><td>—</td><td>SEG3</td><td>—</td><td>P83</td><td></td></tr>
<tr><td>53</td><td>P84/ SEG4</td><td>P84</td><td>—</td><td>SEG4</td><td>—</td><td>P84</td><td></td></tr>
<tr><td>54</td><td>P85/ SEG5</td><td>P85</td><td>—</td><td>SEG5</td><td>—</td><td>P85</td><td></td></tr>
<tr><td>55</td><td>P86/ SEG6</td><td>P86</td><td>—</td><td>SEG6</td><td>—</td><td>P86</td><td></td></tr>
<tr><td>56</td><td>P87/ SEG7</td><td>P87</td><td>—</td><td>SEG7</td><td>—</td><td>P87</td><td></td></tr>
<tr><td>57</td><td>P90/ SEG8</td><td>P90</td><td>—</td><td>SEG8</td><td>—</td><td>P90</td><td></td></tr>
<tr><td>58</td><td>P91/ SEG9</td><td>P91</td><td>—</td><td>SEG9</td><td>—</td><td>P91</td><td></td></tr>
<tr><td>59</td><td>P92/ SEG10</td><td>P92</td><td>—</td><td>SEG10</td><td>—</td><td>P92</td><td></td></tr>
<tr><td>60</td><td>P93/ SEG11</td><td>P93</td><td>—</td><td>SEG11</td><td>—</td><td>P93</td><td></td></tr>
<tr><td>61</td><td>P94/ SEG12</td><td>P94</td><td>—</td><td>SEG12</td><td>—</td><td>P94</td><td></td></tr>
<tr><td>62</td><td>P95/ SEG13</td><td>P95</td><td>—</td><td>SEG13</td><td>—</td><td>P95</td><td></td></tr>
<tr><td>63</td><td>P96/ SEG14</td><td>P96</td><td>—</td><td>SEG14</td><td>—</td><td>P96</td><td></td></tr>
</table>

Note : P : Port selected, F : Specified function selected

(Continued)

Pin no.	Pin name	Port name	Specified function name			At initializing		At sleep mode	At Stop mode		Re-marks
			Input	Output	Input/ Output	Function name	Reset initialization		HIZ = 0	HIZ = 1	
64	P97/ SEG15	P97	—	SEG15	—	P97	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state	
65	PA0/ SEG16	PA0	—	SEG16	—	PA0					
66	PA1/ SEG17	PA1	—	SEG17	—	PA1					
67	PA2/ SEG18	PA2	—	SEG18	—	PA2					
68	PA3/ SEG19	PA3	—	SEG19	—	PA3					
69	PA4/ SEG20	PA4	—	SEG20	—	PA4					
70	PA5/ SEG21	PA5	—	SEG21	—	PA5					
71	PA6/ SEG22	PA6	—	SEG22	—	PA6					
72	PA7/ SEG23	PA7	—	SEG23	—	PA7					
73	PB0/ SEG24	PB0	—	SEG24	—	PB0					
74	PB1/ SEG25	PB1	—	SEG25	—	PB1					
75	V_{CC}	—	—	—	—	—	—	—	—	—	
76	V_{SS}	—	—	—	—	—	—	—	—	—	
77	PB2/ SEG26	PB2	—	SEG26	—	PB2	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state	
78	PB3/ SEG27	PB3	—	SEG27	—	PB3					
79	P64/ SEG28	P64	—	SEG28	—	P64					open-drain pin, I_{OL} = 20 mA

Note : P : Port selected, F : Specified function selected

(Continued)

<table>
<tr><th rowspan="2">Pin no.</th><th rowspan="2">Pin name</th><th rowspan="2">Port name</th><th colspan="3">Specified function name</th><th colspan="2">At initializing</th><th rowspan="2">At sleep mode</th><th colspan="2">At Stop mode</th><th rowspan="2">Re-marks</th></tr>
<tr><th>Input</th><th>Output</th><th>Input/ Output</th><th>Function name</th><th>Reset initialization</th><th>HIZ = 0</th><th>HIZ = 1</th></tr>
<tr><td>80</td><td>P65/ SEG29</td><td>P65</td><td>—</td><td>SEG29</td><td>—</td><td>P65</td><td rowspan="7">Output Hi-Z/ Input enabled</td><td rowspan="7">Retention of the immediately prior state</td><td rowspan="7">Retention of the immediately prior state</td><td rowspan="7">P : Output Hi-Z/ Input 0 fixed
F : Retention of the immediately prior state</td><td>open-drain pin, I_{OL} = 20 mA</td></tr>
<tr><td>81</td><td>P66/ SEG30</td><td>P66</td><td>—</td><td>SEG30</td><td>—</td><td>P66</td><td>open-drain pin, I_{OL} = 20 mA</td></tr>
<tr><td>82</td><td>P67/ SEG31</td><td>P67</td><td>—</td><td>SEG31</td><td>—</td><td>P67</td><td>open-drain pin, I_{OL} = 20 mA</td></tr>
<tr><td>83</td><td>P70/ COM0</td><td>P70</td><td>—</td><td>COM0</td><td>—</td><td>P70</td><td></td></tr>
<tr><td>84</td><td>P71/ COM1</td><td>P71</td><td>—</td><td>COM1</td><td>—</td><td>P71</td><td></td></tr>
<tr><td>85</td><td>P72/ COM2</td><td>P72</td><td>—</td><td>COM2</td><td>—</td><td>P72</td><td></td></tr>
<tr><td>86</td><td>P73/ COM3</td><td>P73</td><td>—</td><td>COM3</td><td>—</td><td>P73</td><td></td></tr>
<tr><td>87</td><td>MOD2</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>88</td><td>MOD1</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>89</td><td>MOD0</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>90</td><td>$\overline{\text{INIT}}$</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>91</td><td>V0</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>92</td><td>V1</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>93</td><td>V2</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
<tr><td>94</td><td>V3</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td></td></tr>
</table>

Note : P : Port selected, F : Specified function selected

(Continued)

Pin no.	Pin name	Port name	Specified function name			At initializing		At sleep mode	At Stop mode		Remarks
			Input	Output	Input/ Output	Function name	Reset initialization		HIZ = 0	HIZ = 1	
95	P00/ SIN0	P00	SIN0	—	—	P00					
96	P01/ SOT0	P01	—	SOT0	—	P01					
97	P02/ SCK0	P02	—	—	SCK0	P02					
98	P03/ SIN1	P03	SIN1	—	—	P03			Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
99	P04/ SOT1	P04	—	SOT1	—	P04					
100	P05/ SCK1	P05	—	—	SCK1	P05	Output Hi-Z/ Input enabled	Retention of the immediately prior state			
101	P06/ IC0	P06	IC0	—	—	P06					
102	P07/ IC1	P07	IC1	—	—	P07					
103	P10/ INT0	P10	INT0	—	—	P10			P : Retention of the immediately prior state F : Input enabled	P : Output Hi-Z F : Input enabled	Pull-up options can be selected
104	P11/ INT1	P11	INT1	—	—	P11					Pull-up options can be selected
105	V_{CC}	—	—	—	—	—	—	—	—	—	
106	V_{SS}	—	—	—	—	—	—	—	—	—	
107	X1	—	—	—	—	—	—	—	—	—	
108	X0	—	—	—	—	—	—	—	—	—	

Note : P : Port selected, F : Specified function selected

(Continued)

(Continued)

Pin no.	Pin name	Port name	Specified function name			At initializing		At sleep mode	At Stop mode		Remarks
			Input	Output	Input/ Output	Function name	Reset initialization		HIZ = 0	HIZ = 1	
109	P12/ INT2	P12	INT2	—	—	P12	Output Hi-Z/ Input enabled	Retention of the immediately prior state	P : Retention of the immediately prior state F : Input enabled	P : Output Hi-Z F : Input enabled	Pull-up options can be selected
110	P13/ INT3	P13	INT3	—	—	P13					Pull-up options can be selected
111	P14/ INT4	P14	INT4	—	—	P14					Pull-up options can be selected
112	P15/ INT5	P15	INT5	—	—	P15					Pull-up options can be selected
113	P16/ INT6	P16	INT6	—	—	P16					Pull-up options can be selected
114	P17/ INT7	P17	INT7	—	—	P17					Pull-up options can be selected
115	P20/ CKI0/ OP0	P20	CKI0	OP0	—	P20			Retention of the immediately prior state	Output Hi-Z/ Input 0 fixed	
116	P21/ CKI1/ OP1	P21	CKI1	OP1	—	P21					
117	P22/ PWI0/ OP2	P22	PWI0	OP2	—	P22					
118	P23/ PWI1/ OP3	P23	PWI1	OP3	—	P23					
119	P24/ SIN2	P24	SIN2	—	—	P24					
120	P25/ SOT2	P25	—	SOT2	—	P25					

Note : P : Port selected, F : Specified function selected

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

MB91F233, MB91V230

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*	V_{CC}	V_{SS}–0.5	V_{SS} + 6.0	V	
	$V_{CC}3$	V_{SS}–0.5	V_{SS} + 4.0	V	
	$V_{CC}3IO$	V_{SS}–0.5	V_{SS} + 4.0	V	
Analog power supply voltage*	AV_{CC}	V_{SS}–0.5	V_{SS} + 4.0	V	
Input voltage*	VI	V_{SS}–0.5	V_{CC} + 0.5	V	
Input voltage* (open-drain)	VIND	V_{SS}–0.5	V_{CC} + 0.5	V	
Analog pin input voltage*	VIA	V_{SS}–0.5	AV_{CC} + 0.5	V	
Output voltage*	VO	V_{SS}–0.5	V_{CC} + 0.5	V	
Operating ambient temperature	Ta	–40	+ 85	°C	
Storage temperature	Tstg	–55	+ 125	°C	

* : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

MB91F233L, MB91233L

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*	V_{CC}	V_{SS}–0.5	V_{SS} + 4.0	V	
	$V_{CC}3$	V_{SS}–0.5	V_{SS} + 4.0	V	
	$V_{CC}3IO$	V_{SS}–0.5	V_{SS} + 4.0	V	
Analog power supply voltage*	AV_{CC}	V_{SS}–0.5	V_{SS} + 4.0	V	
Input voltage*	VI	V_{SS}–0.5	V_{CC} + 0.5	V	
Input voltage* (open-drain)	VIND	V_{SS}–0.5	V_{CC} + 0.5	V	
Analog pin input voltage*	VIA	V_{SS}–0.5	AV_{CC} + 0.5	V	
Output voltage*	VO	V_{SS}–0.5	V_{CC} + 0.5	V	
Operating ambient temperature	Ta	–40	+ 85	°C	
Storage temperature	Tstg	–55	+ 125	°C	

* : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

MB91F233, MB91V230

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Operating ambient temperature	Ta	–40	+ 85	°C	
Power supply voltage	V_{CC}	4.00	5.25	V	*1
	$V_{CC}3$	3.00	3.60	V	*4
	$V_{CC}3B$	3.00	3.60	V	
		2.20	3.60	V	*2
	$V_{CC}3IO$	3.00	3.60	V	
Analog power supply voltage	AV_{CC}	3.00	3.60	V	
LCD reference voltage	V3	—	5.25	V	*3

MB91F233L, MB91233L

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Operating ambient temperature	Ta	–40	+ 85	°C	
Power supply voltage	V_{CC}	3.00	3.60	V	*1
	$V_{CC}3$	3.00	3.60	V	*4
	$V_{CC}3B$	3.00	3.60	V	
		2.20	3.60	V	*2
	$V_{CC}3IO$	3.00	3.60	V	
Analog power supply voltage	AV_{CC}	3.00	3.60	V	
LCD reference voltage	V3	—	3.60	V	*3

*1 : The standard power-supply voltage varies with the model of product.

*2 : Only for backup. Set $V_{CC}3$ = AV_{CC} = $V_{CC}3IO$.

*3 : V3 must not exceed V_{CC}.

*4 : For the relationships between $V_{CC}3$ and operating frequencies, see section “4. AC Characteristics (4) Operation Assurance Range”.
For the MB91V230, please inquire separately.

Note : For normal use, set $V_{CC}3$ = $V_{CC}3B$ = AV_{CC} = $V_{CC}3IO$.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

MB91V230, MB91F233

(V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	I_{CC}	$V_{CC}3$	FLASH model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 16.5 MHz	—	65	75	mA	
			FLASH model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 33 MHz	—	73	83	mA	
	I_{CCT}		RTC mode, @Ta = +25 °C, F_{CP} = 32 kHz	—	20	50	µA	Watch timer, RTC, LCDC $V_{CC}3$ = $V_{CC}3B$ = 2.4 V
	I_{CCH}		STOP mode, @Ta = +25 °C, F_{CP} = 0 kHz	—	5	50	µA	
	I_{CCS}		SLEEP mode F_{CP} = 33 MHz, F_{CPP} = 16.5 MHz	—	21	25	mA	
			SLEEP mode F_{CP} = 33 MHz, F_{CPP} = 33 MHz	—	30	35	mA	
"H" level input voltage	V_{IH}	—	—	V_{CC} × 0.8	—	V_{CC}	V	
		X0A	$V_{CC}3B$ = 2.2 V to 3.6 V	$V_{CC}3B$ × 0.8	—	$V_{CC}3B$	V	When external clock is used
“L” level input voltage	V_{IL}	—	—	V_{SS}	—	V_{CC} × 0.2	V	
		X0A	$V_{CC}3B$ = 2.2 V to 3.6 V	V_{SS}	—	V_{SS} + 0.4	V	When external clock is used
"H" level output voltage	V_{OH}	—	I_{OH} = –4 mA	V_{CC} –0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}	—	I_{OL} = 4 mA	V_{SS}	—	0.4	V	
		P64 to 67	I_{OL} = 20 mA					
Input leakage current	I_{IL}	—	—	–5	—	5	µA	
Open-drain output leakage current	Ileak	—	—	–10	—	10	µA	

(Continued)

(Continued)

(V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCD division resistance	R_{LCD}	V0 - V1, V1 - V2, V2 - V3	—	50	100	200	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
SEG00 to SEG31 output impedance	R_{VSEG}	SEG00 to SEG31		—	—	15	kΩ	
LCDC leakage current	I_{LCDC}	V0 to V3, COM0 to COM3, SEG00 to SEG31	—	–5	—	5	µA	

MB91F233L, MB91233L

(V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	Vcc3	FLASH model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 16.5 MHz	—	65	75	mA	
			FLASH model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 33 MHz	—	73	83	mA	
	I_{CC}		ROM model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 16.5 MHz	—	45	55	mA	
			ROM model normal operation, Ta = +25 °C, F_{CP} = 33 MHz, F_{CPP} = 33 MHz	—	55	65	mA	
	I_{CCT}		RTC mode, @Ta = +25 °C, F_{CP} = 32 kHz	—	20	50	µA	Watch timer, RTC, LCDC $V_{CC}3$ = $V_{CC}3B$ = 2.4 V
	I_{CCH}		STOP mode, @Ta = +25 °C, F_{CP} = 0 MHz	—	5	50	µA	
	I_{CCS}		SLEEP mode F_{CP} = 33 MHz, F_{CPP} = 16.5 MHz	—	21	25	mA	
			SLEEP mode F_{CP} = 33 MHz, F_{CPP} = 33 MHz	—	30	35	mA	
"H" level input voltage	V_{IH}	—	—	V_{CC} × 0.8	—	V_{CC}	V	
		X0A	$V_{CC}3B$ = 2.2 V to 3.6 V	$V_{CC}3B$ × 0.8	—	$V_{CC}3B$	V	When external clock is used
"L" level input voltag	V_{IL}	—	—	V_{SS}	—	V_{CC} × 0.15	V	
		X0A	$V_{CC}3B$ = 2.2 V to 3.6 V	V_{SS}	—	V_{SS} + 0.4	V	When external clock is used
"H" level output voltage	V_{OH}	—	V_{CC} = 3.3 V, I_{OH} = −2 mA	V_{CC} −0.5	—	V_{CC}	V	

(Continued)

(Continued)

(V_{CC} = V_{CC}3 = V_{CC}3B = V_{CC}3IO = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL}	—	I_{OL} = 2 mA	V_{SS}	—	0.4	V	
		P64 to 67	I_{OL} = 10 mA					
Input leakage current	I_{IL}	—	—	–5	—	5	µA	
Open-drain output leakage current	Ileak	—	—	–10	—	10	µA	
LCD division resistance	R_{LCD}	V0 - V1, V1 - V2, V2 - V3	—	50	100	200	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
SEG00 to SEG31 output impedance	R_{VSEG}	SEG00 to SEG31		—	—	15	kΩ	
LCDC leakage current	I_{LCDC}	V0 to V3, COM0 to COM3, SEG00 to SEG31	—	–5	—	–5	µA	

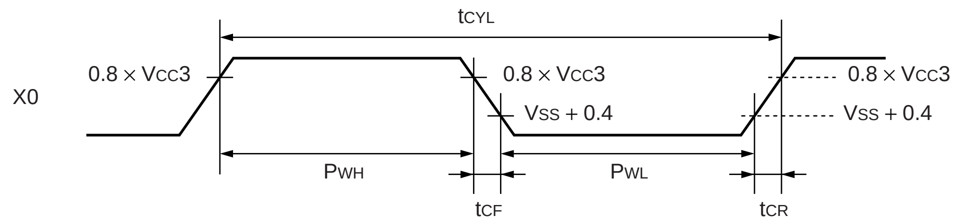
4. AC Characteristics

(1) Main clock input standard

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_C	X0	—	3.6	4	4.2	MHz	
Input clock cycle	t_{CYL}	X0	—	—	250	—	ns	
Input clock pulse width	—	X0	P_{WH}/t_{CYL} P_{WL}/t_{CYL}	40	—	60	%	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	—	—	—	5	ns	At external clock
Internal operating clock frequency	F_{CP}	—	—	—	—	33.6	MHz	
Internal operating clock cycle time	t_{CP}	—	—	29.7	—	—	ns	
Peripheral clock frequency	F_{CPP}	—	—	—	—	33.6	MHz	Peripheral clock is derived from internal operating clock divided by 1/1 to 1/16.
Peripheral clock cycle time	t_{CYCP}	—	—	29.7	—	—	ns	

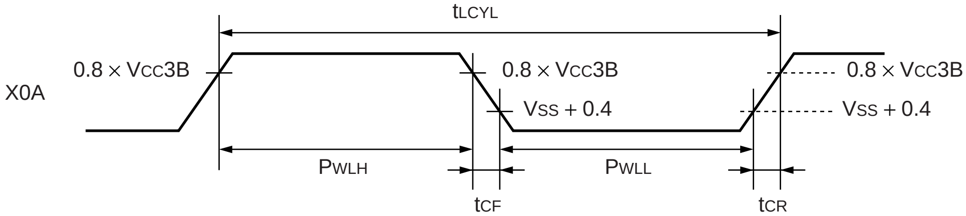


(2) Subclock input standard

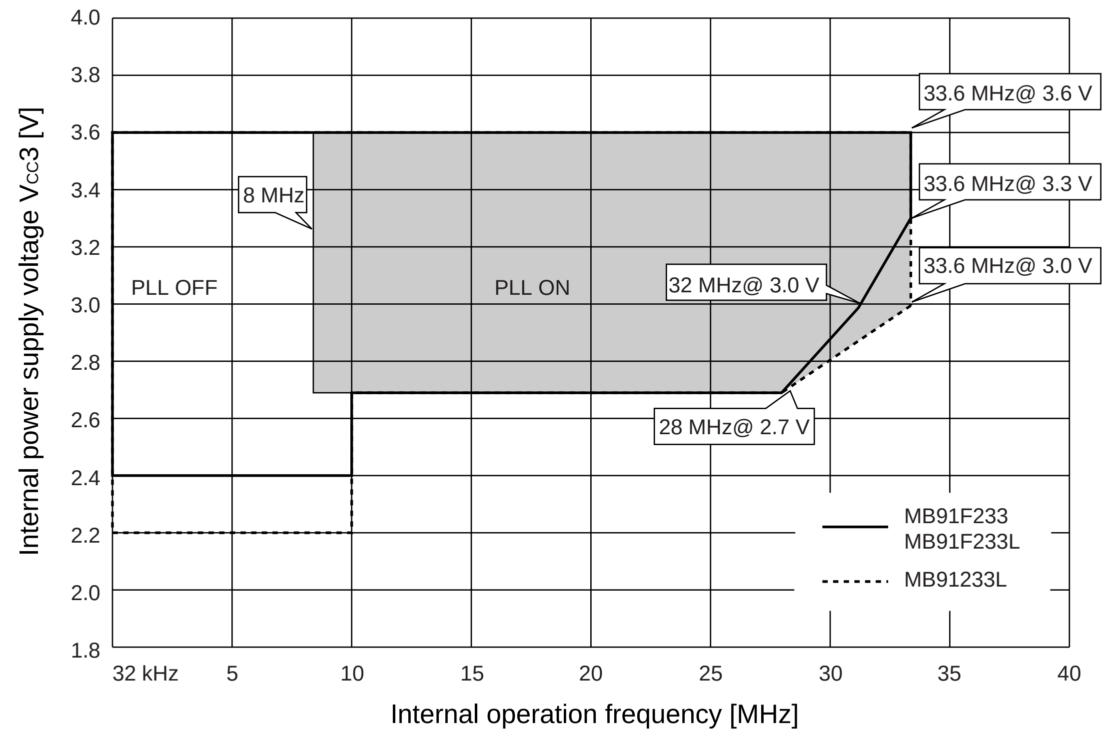
(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A	—	—	32.768	—	kHz	
				28.571	32.768	35.714		At external clock
Input clock cycle	t_{LCYL}		—	28.0	—	35.0	µs	
Input clock pulse width	—		P_{WLH}/t_{LCYL} P_{WLL}/t_{LCYL}	45	—	55	%	
Input clock rise time and fall time	—		t_{CR}/t_{LCYL} t_{CF}/t_{LCYL}	—	—	5	%	At external clock



(3) Operation Assurance Range



(4) PLL oscillation stabilization time (LOCK UP time)

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)
(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	value		Unit	Remarks
		Min	Max		
PLL oscillation stabilization (LOCK UP time)	t_{LOCK}	500	—	µs	Time from when the PLL starts operating to when its oscillation becomes stable

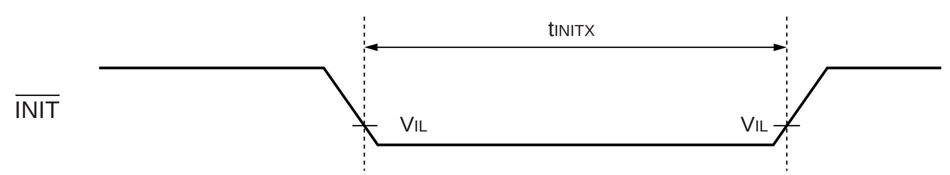
(5) Reset input standards

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)
(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time (at power-on)	t_{INITX}	$\overline{INIT}$	—	—	—	ns	*1
Reset input time (other than at power-on)	t_{INITX}	$\overline{INIT}$	—	t_{CP} × 10	—	ns	*2

*1 : When turning the power on, keep $\overline{INIT}$ input until the oscillation circuit provides stable oscillation.

*2 : t_{CP} indicates cycle time of CPU operating clock.



(6)UART timing

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

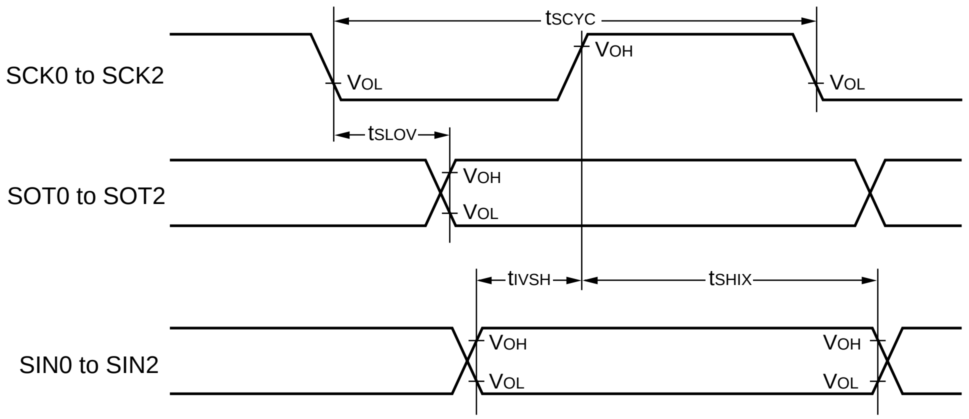
(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock operation	8 t_{CYCP} *	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock operation	4 t_{CYCP} *	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CYCP}*	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

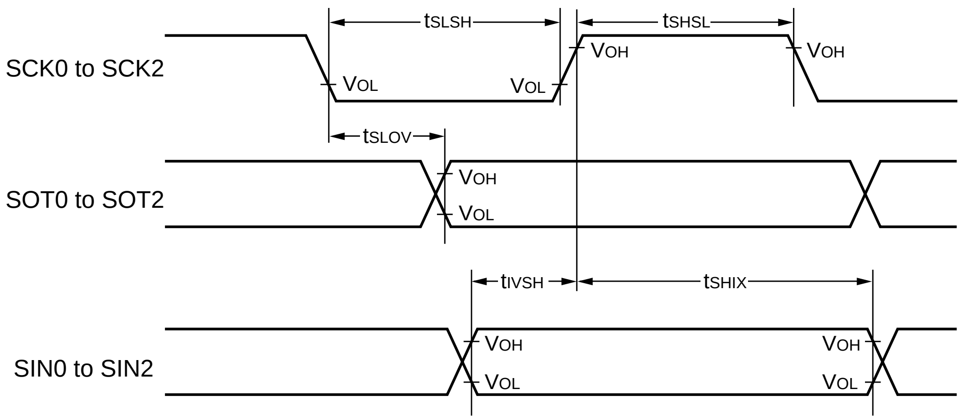
* : t_{CYCP} represents the cycle time of peripheral operating clock.

Note : This specification applies to clock synchronous mode operation.

• Internal shift clock mode



• External shift clock mode

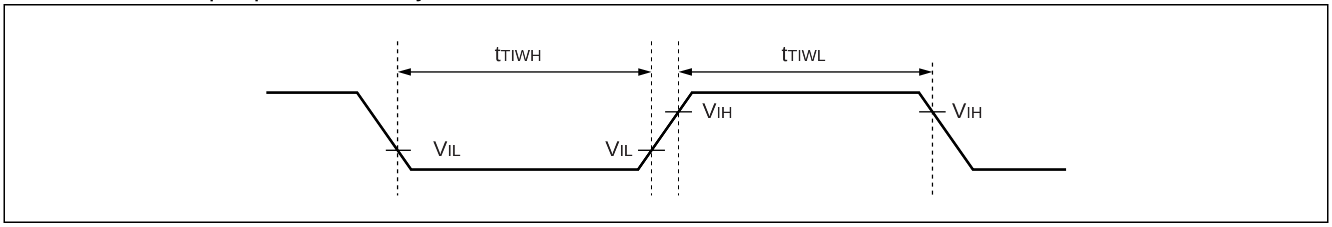


(7) Free-run timer clock, Reload timer event input, Up/down counter input, Input capture input, Interrupt input timing

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to + 85 °C)
(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulth width	t_{TIWH} t_{TIWL}	CKI0, CKI1 TIN0, TIN1, TIN2 IC0, IC1 AIN0, AIN1 BIN0, BIN1 ZIN0, ZIN1	—	t_{CYCP} × 2	—	ns	*
		INT0 to INT15		t_{CYCP} × 3	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.

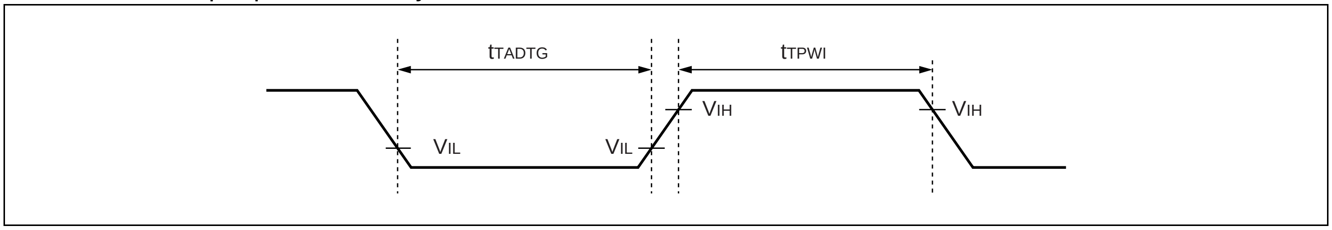


(8) A/D trigger, PWI (PWC) input timing

(MB91V230, MB91F233 : V_{CC} = 4.0 V to 5.25 V, $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to + 85 °C)
(MB91F233L, MB91233L : V_{CC} = $V_{CC}3$ = $V_{CC}3B$ = $V_{CC}3IO$ = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
A/D trigger input (falling)	t_{TADTG}	ADTG0 ADTG1	—	t_{CYCP} × 2	—	ns	*
PWI (PWC) input (rising)	t_{PWI}	PWI0, PWI1	—	t_{CYCP} × 2	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.



5. Electrical Characteristics for the A/D Converter

($V_{CC}3IO = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, AVRH = 3.0 V to 3.6 V, Ta = 0 °C to +85 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	$AV_{CC} = 3.3$ V, At AVRH = 3.3 V At CPU sleep mode
Total error*1	–5.0	—	+5.0	LSB	
Nonlinear error*1	–3.5	—	+3.5	LSB	
Differential linear error*1	–2.5	—	+2.5	LSB	
Zero transition voltage*1	–2.0	+1.0	+6.0	LSB	
Full transition voltage*1	AVRH–5.5	AVRH–1.0	AVRH+3.0	LSB	
Conversion time	1.69*2	—	—	µs	
Power supply voltage (analog+digital)	—	3.6	—	mA	
	—	—	5	µA	
Reference power supply current (between AVRH and AVRL)	—	470	—	µA	AVRH = 3.0 V, At AVRL = 0.0 V*3
	—	—	10	µA	At power-down*4
Analog input capacitance	—	40	—	pF	
Inter-channel disparity	—	—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : It depends on the clock cycle supplied to peripheral resources.

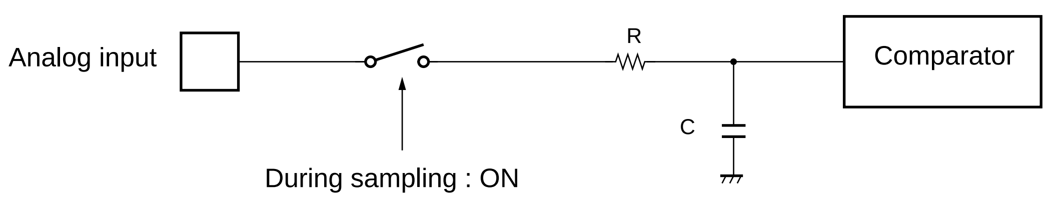
*3 : AVRL pin is only for FLGA package product. AVRL pin is connected to AV_{SS} inside the IC on QFP package product.

*4 : The current when the CPU is in stop mode and the A/D converter is not operaring.

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• Analog input circuit model

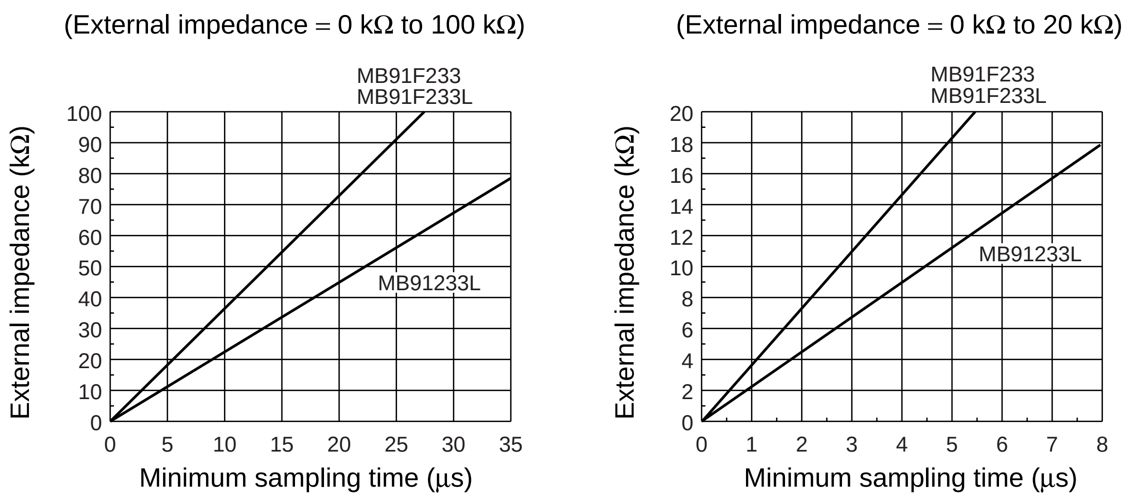


	R	C
MB91233L	0.18 kΩ (Max)	63.0 pF (Max)
MB91F233	0.18 kΩ (Max)	39.0 pF (Max)
MB91F233L	0.18 kΩ (Max)	39.0 pF (Max)

Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

• The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- About errors

  As |AVRH – AV_{SS}| becomes smaller, values of relative errors grow larger.

6. Electrical Characteristics for the D/A Converter

($V_{CC}3IO = AV_{CC} = 3.0$ V to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, Ta = 0 °C to +85 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	8	bit	
Nonlinear error	–2.0	—	+2.0	LSB	When the output is unloaded
Differential linear error	–1.0	—	+1.0	LSB	When the output is unloaded
Conversion speed	—	0.6	—	µs	When load capacitance (C_L) = 20 pF
	—	3.0	—	µs	When load capacitance (C_L) = 100 pF
Output impedance	2.0	2.9	3.8	kΩ	
Analog current	—	40	—	µA	10 µs conversion, when the output is unloaded
	—	—	460*	µA	When the input digital code is fixed at $7A_H$ or 85_H
	—	0.1	—	µA	At power-down

* : The current consumption by this D/A converter varies with input digital code.
  This standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

7. Flash Memory Write/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Ta = + 25 °C, Vcc = 5.0 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time	Ta = + 25 °C, Vcc = 5.0 V	—	10	—	s	Excludes 00_H programming prior erasure
Byte write time	Ta = + 25 °C, Vcc = 5.0 V	—	8	3,600	µs	Not including system-level overhead time.
Chip write time	Ta = + 25 °C, Vcc = 5.0 V	—	2.1	—	s	Not including system-level overhead time.
Erase/write cycle	—	10,000	—	—	cycle	
Flash data retention time	Average Ta = + 85 °C	20	—	—	year	*

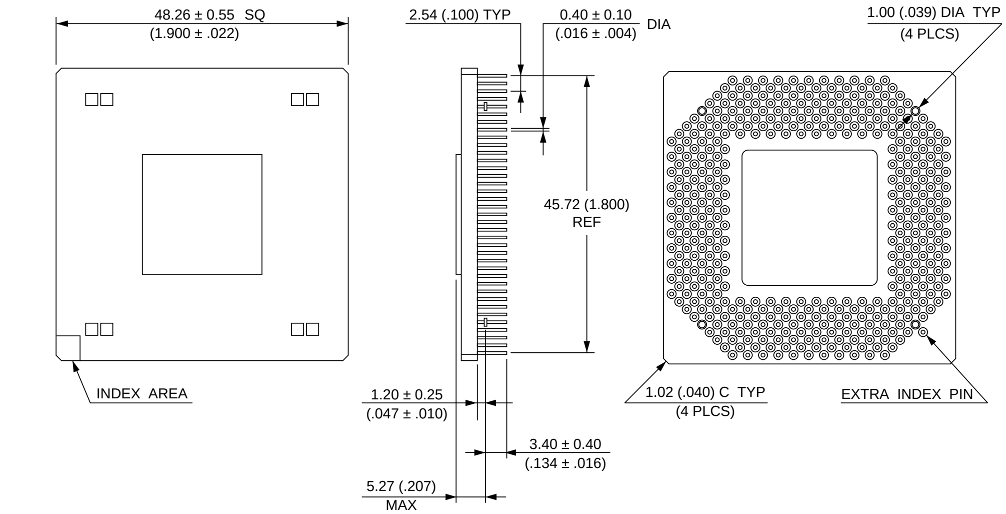
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB91V230CR-ES	401-pin ceramic PGA (PGA-401C-A02)	
MB91F233PFF-GE1	120-pin plastic LQFP (FPT-120P-M05)	
MB91F233LPFF-GE1	120-pin plastic LQFP (FPT-120P-M05)	
MB91F233LLGA-GE1	128-pin plastic FLGA (LGA-128P-M01)	
MB91233LPFF-G-xxx-BNDE1	120-pin plastic LQFP (FPT-120P-M05)	
MB91233LLGA-Gxxx-BNDE1	128-pin plastic FLGA (LGA-128P-M01)	

■ PACKAGE DIMENSIONS

401-pin Ceramic PGA
(PGA-401C-A02)

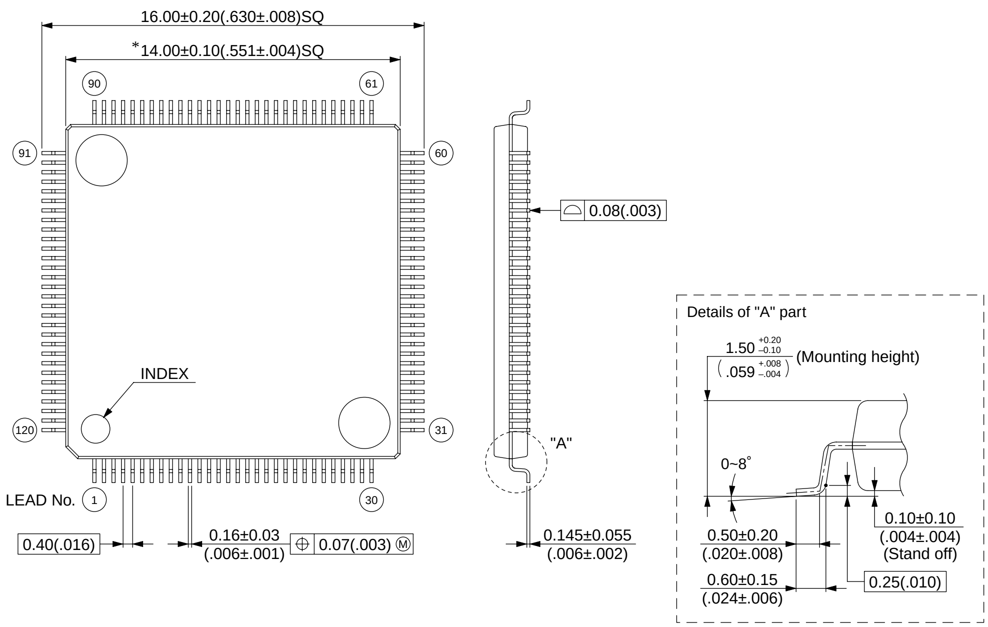


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

120-pin Plastic LQFP
(FPT-120P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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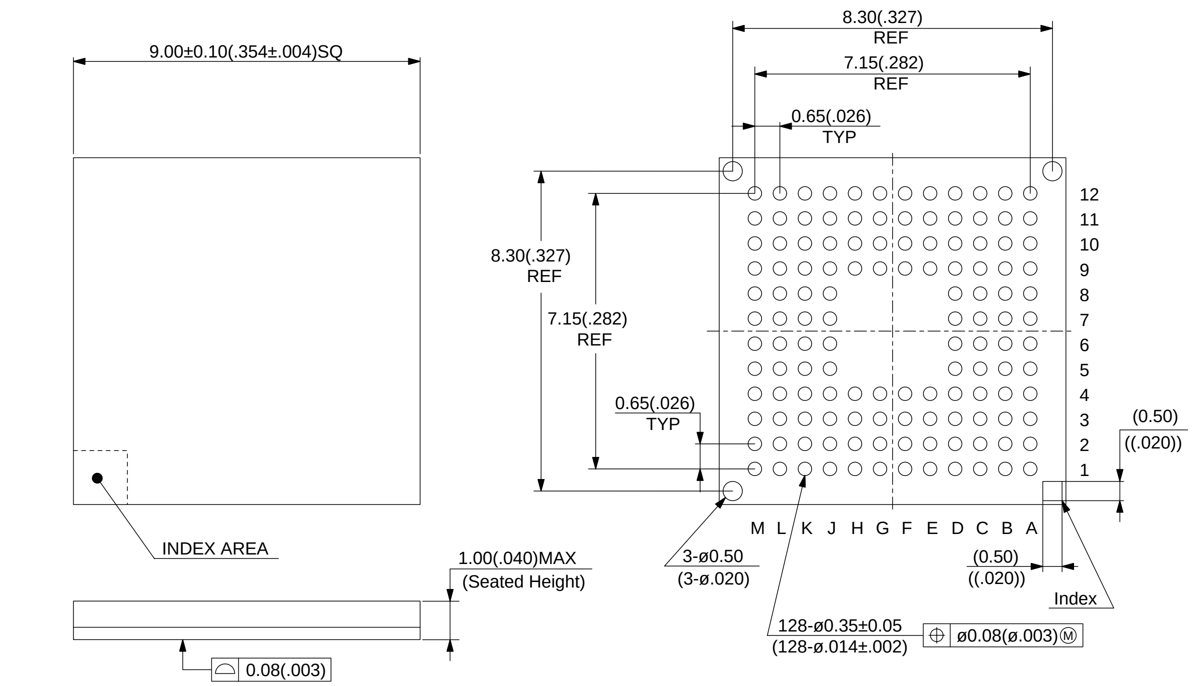
128-pin plastic FLGA
(LGA-128P-M01)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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